

---

# Passivation and characterization of hyper-uniform disordered thin-film silicon solar cells

---

**Jelena Dolecek**  
– 248106 –

Master Thesis

Master of Science and Engineering  
(M.Sc.)

Materials Science and Engineering

Handed in on the 27<sup>th</sup> of August 2021

*at*

Institute of physics of functional complex matter (AMOLF)

*and*

Ecole Polytechnique Fédérale de Lausanne (EPFL)

**Supervisor AMOLF** Dr. Esther Alarcon Llado  
**Supervisor EPFL** Dr. Anna Fontcuberta i Morral



# Abstract

---

The importance and efficiency of surface passivation for ultrathin-silicon technology with high-aspect ratio structures need to be understood and tested in order to fully explore their potential as cost-efficient, mechanically flexible and transparent solar cells. The aim of this project is to deposit, characterize and understand common passivation techniques applied on hyper-uniform disordered (HUD) structured thin-Si and eventually transfer the process on thinned-down IBC solar cells. Samples were produced with Substrate Conformal Imprint Lithography (SCIL). Electrochemical impedance spectroscopy (EIS) was implemented for Interface trap density measurements. Minority charge carrier lifetimes and absorbance data was collected for various passivation and patterning schemes on thick and thin silicon samples. An important density of interface traps states has been observed for all samples. No conclusion about the effect of different passivation approaches on the interface trap states and lifetimes could yet been drawn.



# Acknowledgments

---

I would like to thank Esther for giving me the opportunity to join the group and all the constructive advice during my stay. I am grateful to the whole team for the stimulating and welcoming atmosphere. Especially Daphne and Yorick, who were always available for discussions that exceeded their domain of expertise and stayed until the end. Furthermore, I'd like to acknowledge the great preliminary work accomplished by Nasim, Stefan and Alex, that made the immersion into HUD solar cells very inspiring. This collaboration was greatly supported by Albert, coordinating the collective efforts and giving me personal guidance. Thanks as well to the NanoLab, Amsterdam, staff who were supportive with training and general advice. I'm grateful to Eitan and Susan for their patient discussion about UV-VIS modifications, and generally all the collaborators at AMOLF, who make research at this institution an inclusive and collaborative experience. Work at AMOLF was great even during these special times and a feeling of belonging was transmitted from the very beginning. Further, I'm grateful to Petra Manshanden and Fatemeh Manaye from TNO, Petten, to give me valuable support for PL measurements. Last but not least, thanks a lot to Anna Fontcuberta i Morral for encouraging and supporting this project abroad regardless of the current sanitary situation.



# Contents

---

<b>Abstract</b>	<b>iii</b>
<b>Acknowledgments</b>	<b>v</b>
<b>Contents</b>	<b>vii</b>
<b>1 Introduction</b>	<b>1</b>
1.1 Introduction . . . . .	1
1.2 Thin-film solar cells . . . . .	2
1.2.1 Limits and potential of thin-film silicon solar cells . . . . .	2
1.2.2 Light-trapping in solar cells . . . . .	4
1.2.3 Surface quality: critical parameters . . . . .	5
1.3 Passivation of thin silicon . . . . .	7
1.3.1 Silicon Dioxide . . . . .	8
1.3.2 Silicon nitride . . . . .	8
1.3.3 Alumina + annealing . . . . .	9
1.3.4 Titanium Dioxide . . . . .	10
1.3.5 Combinations: multi-layer passivation . . . . .	10
1.3.6 Passivation and solar cell performance . . . . .	11
1.4 Characterization of thin silicon . . . . .	12
1.4.1 Capacitance methods: MOS devices . . . . .	12
1.4.2 Photoluminescence . . . . .	16
<b>2 Fabrication</b>	<b>17</b>
2.1 Fabrication of HUD thin silicon solar cells . . . . .	17
2.1.1 Bonding and debonding of thin-Si wafers . . . . .	17
2.1.2 Imprinting: SCIL . . . . .	19
2.2 Passivation Techniques . . . . .	20
2.2.1 Deposition of amorphous $\text{Al}_2\text{O}_3$ and annealing . . . . .	20
2.2.2 Deposition of amorphous $\text{SiO}_2$ . . . . .	21
2.2.3 Deposition of $\text{SiN}_x$ . . . . .	21
<b>3 Characterization</b>	<b>23</b>
3.1 Evaluation of optical properties with UV-VIS spectroscopy . . . . .	23
3.1.1 Transmission measurement . . . . .	23

3.1.2	Reflection measurement . . . . .	24
3.1.3	Comparison with analytical results . . . . .	25
3.2	EIS and CV . . . . .	26
3.2.1	Setup and measurement technique . . . . .	26
3.2.2	Analysis of the data . . . . .	27
3.3	Measurement of Interface Traps in silicon using MOS capacitors: the Terman method . . . . .	27
3.3.1	Ideal $\Psi_S$ vs. V curves for the high-frequency Terman method . . .	29
3.4	Lifetimes measurements . . . . .	30
<b>4</b>	<b>Results &amp; Discussion</b>	<b>33</b>
4.1	Fabrication of the samples . . . . .	33
4.1.1	SCIL fabrication and etch parameters . . . . .	33
4.1.2	Passivation of the samples . . . . .	33
4.2	Optical properties and absorption measurements . . . . .	34
4.3	Surface state density measurements . . . . .	38
4.4	Minority carrier lifetimes measurement . . . . .	41
4.5	Terman method and NextNano . . . . .	44
<b>5</b>	<b>Conclusions &amp; Outlook</b>	<b>47</b>
<b>6</b>	<b>Appendix</b>	<b>49</b>
	<b>Bibliography</b>	<b>55</b>
	<b>Declaration of Authorship</b>	<b>59</b>

## 1.1 Introduction

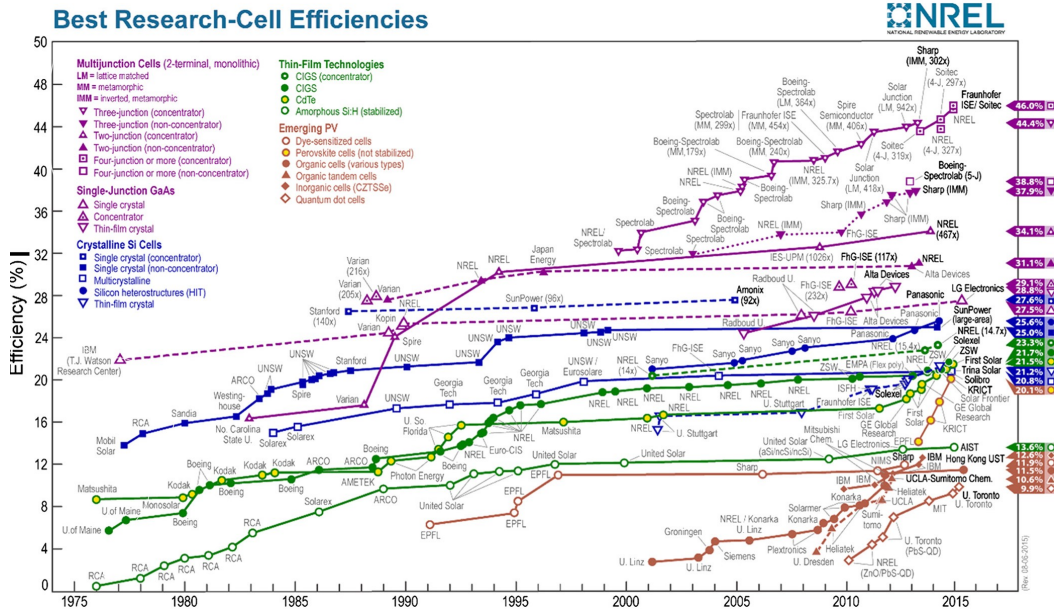
Electricity provided by renewable technologies increased by 6% in 2019 alone and the energy from wind and solar each accounted for one third of the rise. That year renewable power represented 27% of the global electricity supply, with an increasing tendency. Nonetheless, as the new IPCC 2021 report pinpoints clearly, emissions need to be drastically reduced, putting as well more pressure on renewable energies. This sector needs to keep growing annually by at least 7% over the next ten years. By then the solar energy sector alone is envisioned to represent 21.8% of the total global renewable power [18]. This needs to go hand in hand with a renewable energy cost reduction. For moderate radiation areas the cost of PV energy is expected to achieve of fossil fuel by 2028 and 2046 for residential and industrial applications, respectively [15]. This forecast can only be met if efficiencies are further increased and costs reduced.

Solar cells based on single-junction monocrystalline semiconductors have almost reached the Shockley-Queisser (SQ) limit. This is the theoretical maximum light to electric power conversion efficiency of an ideal solar cell under a certain illumination spectrum [35]. Efficiencies of 25% and 20% have been reached for mono- and polycrystalline silicon cells, respectively [15]. These cells are based on the principle of single-pass photons, where incident photons need to be absorbed as efficiently as possible through rather thick absorbers [26]. To overcome the SQ limit and reduce costs, new light trapping and interference strategies are being developed in order to increase the effective path length of the photons, while slimming down simultaneously the absorber layer, but maintaining or even increasing the performance [26].

Crystalline silicon based solar cells represented 90% of the global photovoltaics market over the recent years. The silicon absorber layer alone accounts for about 40% of the final PV cost and reducing its thickness is paramount for cost reduction [39], one of the many benefits of (ultra)thin-Si solar cells. Thinner cells require as well shorter deposition/growth times during production and the use of novel low-cost technologies like chemical vapor deposition may become possible for thin-Si solar cells [26]. In thin absorbers many limitations of bulk semiconductors can be avoided and the efficiency increased. Concerned are namely limitations dominated by recombination processes. In an ideal solar cell (SQ limit), the only recombination mechanism is radiative recombination, excluding the dominant bulk processes which can be limited by thin layers. Aiming for thinner layers paves the path to lighter, mechanically flexible and transparent applications,

opening a new dimension of applications for solar cells [26, 40].

In Figure 1.1 the development of cell-efficiencies is depicted since 1975. Where the crystalline Si Cells have been plateauing since 2000, thin-film technologies, as well as multi-junction cells and new (emerging) technologies, have been continuously increasing. The trend is clear; Improved and new solar conversion technologies are on the rise.



**Figure 1.1:** Solar cell efficiencies per category since 1975, *courtesy of the National Renewable Energy Laboratory, Golden* [29]. Pink: Multi-junction cells, blue: C-Si cells, green: thin-film technologies, brown: emerging PVs.

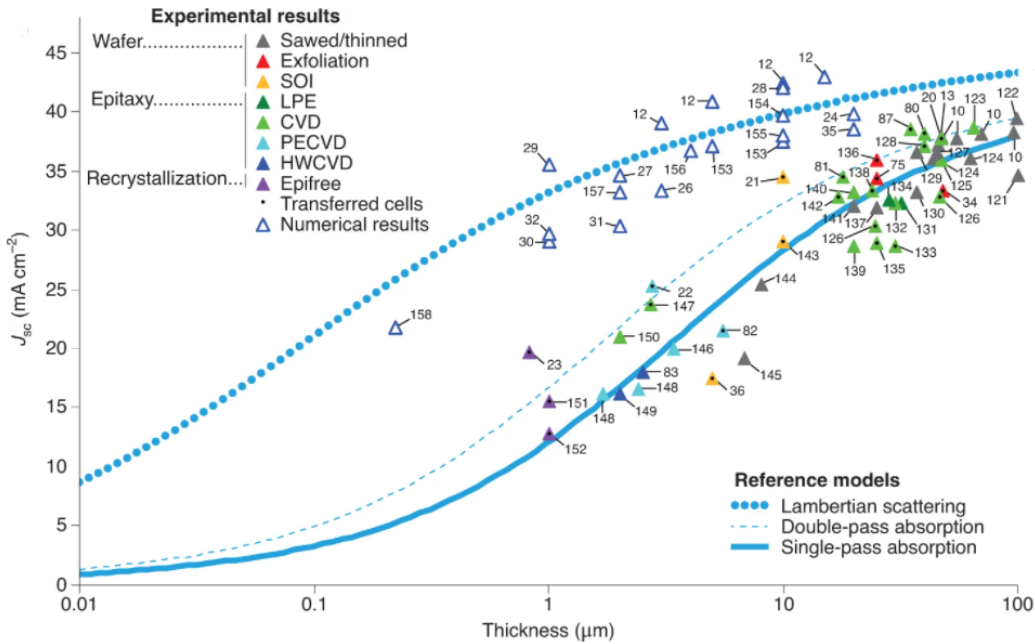
## 1.2 Thin-film solar cells

### 1.2.1 Limits and potential of thin-film silicon solar cells

The SQ limit for a single junction c-Si cell under one sun and at room temperature is of 32.23% [15]. Incomplete absorption of incoming photons and non-radiative recombination of parasitic photogenerated charge carriers (parasitic absorption) make it impossible to reach the limit. As silicon has an indirect band gap, radiation in the range of 800-1100 nm is rather badly absorbed. Richter *et al.* (2013) suggested that the real efficiency limit in practice for an undoped c-Si absorber thickness of 110  $\mu\text{m}$  is 29.43% for perfect Lambertian light trapping [3, 34]. The absorption efficiency is strongly absorber thickness and wavelength dependent. For 2  $\mu\text{m}$  c-Si and in single-pass configuration, only 40% of the

photons with wavelengths above 650 nm are absorbed [26]. Improving the absorption close to the bandgap of 1100 nm is thus crucial in order to further push the absorption efficiency.

Bhattacharya *et al.* (2019) suggest that by including wave-interference corrections in structures at the optical wavelength scale, thin-Si can overcome the theoretical efficiency limits of thick Si cells. The dwell time is much longer in thin-film cells, as wave interference reduces the group velocity [3]. Figure 1.2 shows experimental results for single-pass absorption (ultra-)thin c-Si solar cells and theoretical results based on absorption measurements for nanostructured front surfaces. They suggest that the Lambertian scattering limit can be exceeded by optimized surface structuring. Thinner solar cells have as well reduced electron collection paths which is a promising strategy to reduce bulk recombination and eventually even surface recombination, if the diffusion lengths of the minority charge carriers are larger than the mean path to the contacts [28]. By using IBC contacts, the path of the charge carriers generated at the surface could be short enough to overcome before (surface) recombination occurs.



**Figure 1.2:** Short-circuit current as a measure for the absorption efficiency as a function of the absorber thickness for different crystal growth methods. Filled triangles represent experimental results, empty triangles numerical results (based on absorption measurements). Cells with record efficiencies exceeding the Lambertian limit make use of nanostructured surfaces. *Courtesy of Massiot et al. (2020) [26].*

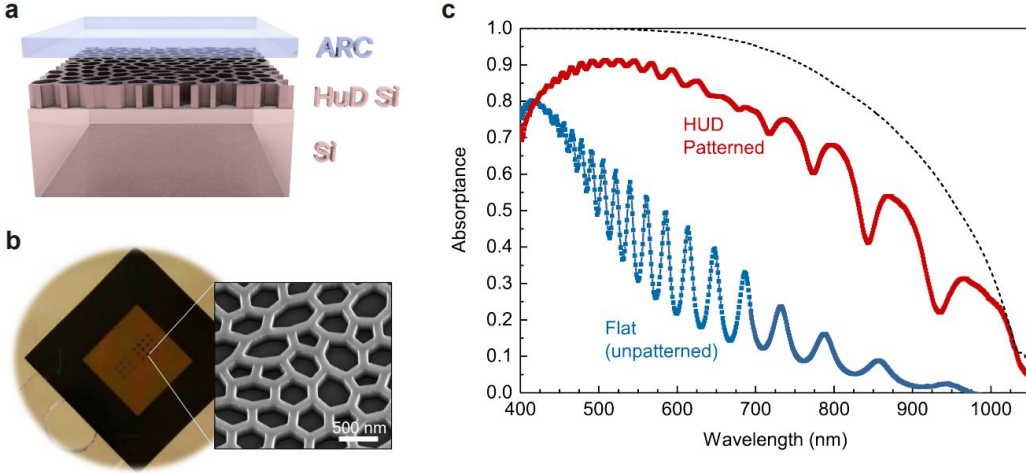
### 1.2.2 Light-trapping in solar cells

The absorption coefficient of the semiconductor depends on intrinsic properties like the complex refractive index and the sheet thickness. The refractive index of silicon is strongly wavelength dependent (appendix, Figure 6.1) and thus is as well the absorption efficiency. The absorption as a function of wavelength is expressed as:  $A(\lambda) = 1 - e^{-\alpha d}$  or  $A(\lambda) = 1 - e^{-F\alpha d}$ , with  $\alpha = 4\pi\kappa/\lambda$  the absorption coefficient and  $F$  the optical path enhancement factor, describing the efficiency of light trapping, increased by resonance for instance [26]. The optical path increase is maximized if the photons are scattered fully randomly upon incidence and internally. This can theoretically be achieved with a back mirror, perfect anti-reflective coating (ARC) and a Lambertian scatterer.

There's thus a big potential to be explored in new light-trapping technologies for ultrathin solar cells by patterning the surface at the nanometer scale. Nanopatterning increases not only the absorption of light, but decreases as well the surface reflectance [28]. With Lambertian light trapping, the currently achieved efficiency of 26% for c-Si solar cells could be obtained with 10  $\mu\text{m}$  c-Si absorbers [26]. Structures resulting in multi-resonant absorption (slow photonic modes) have shown to reach or even exceed the theoretical Lambertian limit over the broad solar spectrum, where  $F$  reached almost maximal enhancement [3, 26]. These technologies are typically the ones shown in Figure 1.2.

Thinning down the absorber comes along with new challenges in the solar cell architecture. Texturing may increase the non-radiative surface recombination or parasitic absorption might occur in contact layers. Selective contacting, ARC and surface passivation may be even important in ultrathin solar cells [26]. Unless, the charge carriers can be collected before recombination due to short distances that need to be overcome till the contacts.

**Hyper-uniform disordered (HUD) thin-Si solar cells** HUD structures are a type of nanotexturing that couple light efficiently into silicon slab optical modes. Over a larger scale, these structures are statistically isotropic and thus not completely random. In terms of density distribution, HUD structures are more similar to ordered solids than amorphous materials. This large-scale isotropy can be applied to photonic materials in order to design properties with well defined photonic gaps that allow modes to propagate through the structure. Ultimately, this allows the a exact control of light transport and optical properties [40]. Tavakoli *et al.* (2020) reported from analytical results that efficiencies above 20% could be reached with a 1  $\mu\text{m}$  HUD structured c-Si absorbers. This is shown in Figure 1.3, c), where the absorbance approaches the Lambertian limit. The theoretical absorbance of the 200 nm deep HUD structures on 1  $\mu\text{m}$  c-Si is suggested to well outperform the flat 1  $\mu\text{m}$  c-Si. The dashed line represents the Lambertian limit for 1  $\mu\text{m}$  c-Si. On Figure 1.3, b) a SEM image of a honeycomb HUD structure is shown and in a) the HUD on top of a thicker c-Si substrate [40].



**Figure 1.3:** a) 200 nm HUD texturing on top of a  $1\ \mu\text{m}$  Si substrate, covered by an polymeric ARC. b) SEM picture of an optimized honeycomb-like HUD texture. c) Absorptance spectrum of the structure contrasted to flat  $1\ \mu\text{m}$  Si, where the dashed line corresponds to the Lambertian limit for the silicon of the same thickness. *Courtesy of Tavakoli et al. (2020) [20].*

The refractive index of the HUD pattern can be approximated by:

$$n_{HUD} \approx n_{Si} \cdot ff + n_{LRM}(1 - ff) \quad (1.1)$$

where  $ff$  is the filling fraction of the pattern,  $n_{Si}$  the refractive index of the silicon substrate and  $n_{LRM}$  the refractive index of the (polymeric) coating that is filling up the free space. For free standing patterns the latter would be the refractive index of air. The main effect of nanostructuring is increased light trapping and but as well increased charge recombination by high surface-volume ratios [40].

### 1.2.3 Surface quality: critical parameters

Micro- and nanostructured c-Si solar cells still haven't reached as high efficiencies as thick absorber cells. This is mainly due to much higher surface recombination velocities originating in the high aspect ratio features and surface-to-volume ratios. Important parameters to estimate properties of the surface are surface recombination velocity, minority charge carrier lifetime and interface trap density [28].

The effective carrier lifetime is the ratio between the excess minority carrier density ( $\Delta p$ ) and the effective recombination rate ( $U_{eff}$ ):  $\tau_{eff} := \Delta p / U_{eff}$ . The effective recombination rate is the sum of all the mechanisms contributing to recombination. When the surface

and bulk mechanisms are considered, the effective carrier lifetime becomes [11]:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_s} \quad (1.2)$$

The recombination lifetime describes the process of a charge in an excited state (in a space-charge region) returning to equilibrium. The lifetimes can be correlated to interface trap state densities, changing the dynamics of charging/decharging. Recombination taking place at the surface is characterized by the surface recombination velocity ( $S_r$ ). Simultaneously, recombination in the bulk occurs and it is difficult to separate their contributions [37]. In ultrathin Si the effective lifetimes measured are dominated by surface recombination.

If the bulk lifetimes are assumed infinite, the maximal effective surface recombination can be expressed as :  $S_r^{max} \leq \frac{W}{2 \cdot \tau_{eff}}$ , where  $W$  the substrate thickness [17].

When silicon is covered by a dielectric, a major discontinuity is introduced between the crystalline semiconductor surface and adjacent layer. This results in an interface trap density ( $D_{it}$ ) and trapped oxide charges ( $Q_{it}$ ), introduced for example by impurities, excess silicon (trivalent) or contrarily dangling Si bonds (broken Si-H bonds). These interface traps are introducing energy levels into the former state-free bandgap of Si. By means of these intermediate energy levels, charges can be exchanged very quickly with the silicon and thus influence its properties. Whereas  $D_{it}$  is produced by the crystalline discontinuity at the surface,  $Q_{it}$  vary with the occupancy of the Fermi level, i.e the applied voltage. The Fermi level changes with respect to the surface trap energies, modifying the charges and the effective surface capacitance. Another type of charges are fixed oxide charges ( $Q_f$ ), which are situated near or at the interface and are not influenced when a voltage is applied [38, 41].

First, the density of interface traps with respect to the location in the band gap and second, the relaxation time of the charges occupying these states, i.e the lifetime [41], are two important parameters in order to quantify and understand the interface traps.

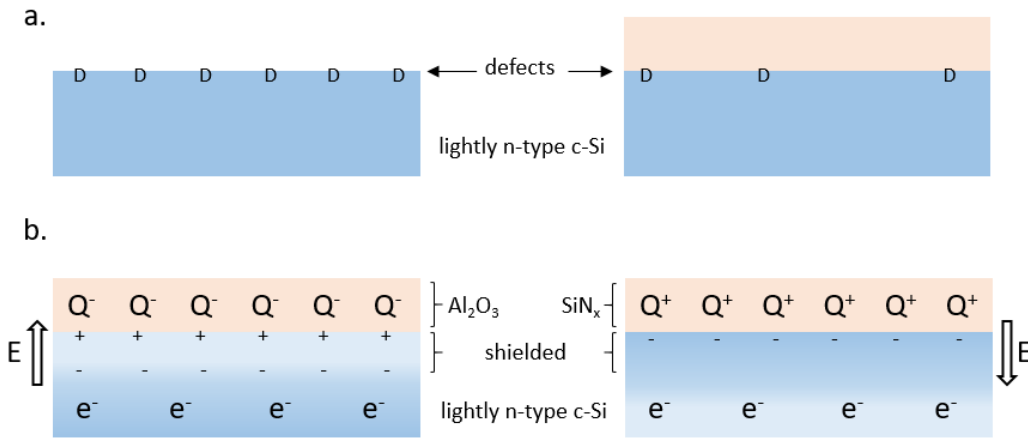
Independently of the nature of the semiconductor, both donor and acceptor interface trap states coexist. Therefore, an equivalent  $D_{it}$  distribution is used with respect to a neutral level  $E_0$ . Above this level the states are of acceptor, below of donor type. In order to determine  $D_{it}$  experimentally, the change of  $Q_{it}$  when varying  $E_F$  or the surface potential  $\Psi_s$  can be measured. The surface trap states are distributed over the band gap and can be described by a density distribution function [38]:

$$D_{it} = \frac{1}{q} \frac{dQ_{it}}{dE} \quad [\#traps/cm^2 eV] \quad (1.3)$$

### 1.3 Passivation of thin silicon

With advancing technology the bulk carrier lifetimes in c-Si have been increasing, making the surface recombination and at the contacts one of the main drawbacks of the current c-Si cells. The surface recombination is not only relatively more important in thin-Si than in bulk Si, but gets even more important in nanostructured surfaces with high surface-to-volume ratios.

The minority carrier lifetimes can be increased by two approaches. The first is based on the reduction of the interface trap state density, the second reduces the electron (n-doped) or hole (p-doped) concentration at the surface in order to decrease the probability of recombination. The former approach is called chemical passivation, the latter field-effect passivation and can be used combined, too [17].



**Figure 1.4:** Passivation schemes for n-type c-Si. a) Chemical passivation in order to decrease the number of defects (D) at the semiconductor surface. b) Field-effect passivation by adding negative fixed-charges ( $Q^-$ ) or positive fixed-charges ( $Q^+$ ) to the semiconductor surface. The electrical field can be strong enough to shield the surface from either electrons (left) or holes (right) for lightly n-doped c-Si.

**Chemical passivation** In order to reduce the number of defects at the surface, chemical passivation can be used to diminish the effect or amount of impurities, trivalent silicon or dangling Si bonds. So can unsaturated Si bonds be stabilized by atomic hydrogen [17]. This is illustrated in Figure 1.4 a, where the defect density (D) is reduced after the application of a passivation layer.

**Field-effect passivation** In order to reduce the probability of recombination at the surface, an electrical field can be applied beneath the silicon surface in order to lower the concentration of holes or electrons at the surface. The minority carrier concentration is directly correlated to the surface recombination velocity [17]. This is depicted in Figure 1.4 b, where either the surface is either shielded from electrons (left) or holes (right), depending on the fixed-charges applied at the surface. In the absence of an additional field, holes are the minority carriers in n-doped, electrons in p-doped. Under strong positive-charge density, holes become the minority charge carriers at the surface for lightly n- and p-doped c-Si. On the contrary, a strong negative-charge density proved to shield the surface efficiently for lightly n- and p-type c-Si as well, hence when the electrons are the minority charge carriers. This is shown in Figure 1.4 b, left, where the electrons added by doping ( $e^-$ ) are still pushed back from the surface. Therefore, efficient field-effect passivation can be obtained by shielding the surface from either electrons or holes, if the fixed-charge density is sufficiently high [17].

### 1.3.1 Silicon Dioxide

Thermally grown  $\text{SiO}_2$  is one of the main industrial approaches to reduce surface recombination velocities. The interface between the silicon dioxide and the silicon is of very good quality, effectively reducing defects at the silicon surface. Further improvements have been reported after annealing in a  $\text{H}_2$  atmosphere, called hydrogenation or *annealing* [9, 17]. Due to high processing temperatures that make the deposition inefficient at industrial scale and require low impurity densities in order to avoid bulk degradation, the thermally grown  $\text{SiO}_2$  has been largely replaced by PECVD grown layers.

Furthermore, apart from the good chemical passivation properties,  $\text{SiO}_2$  has a high positive fixed-charge density and contributes thus as well by field-effect passivation. Zhang *et al.* (2017) did an extensive study on the impact of hydrogen and oxygen incorporation in to the a- $\text{SiO}_x$ . The surface passivation is known to be very good, but important parasitic absorption losses have been observed. Hence, an approach that includes more oxygen into the oxide has been studied lately, in order to reduce the parasitic absorption. Oxygen has a bandgap widening effect on the silicon. They conclude that: "*A compact, less-defective and ordered microstructure of the a-SiO<sub>x</sub>:H film can only be obtained when there comes a trade-off between Si-O and Si-H(Si<sub>3</sub>) bonding formation.*" Controlling the exact composition and adding eventual annealing steps in oxygen or hydrogen atmospheres can be used to further improve the surface passivation quality [43].

### 1.3.2 Silicon nitride

$\text{SiN}_x$  is a standardized approach for surface passivation. Due to high positive fixed charge densities induced in a- $\text{SiN}_x$ :H layers, the hole concentration is reduced at the surface [17]. This makes it very efficient for n-doped c-Si. For the reason explained above, a high

surface passivation can be achieved as well on lightly p-doped c-Si. For both,  $\text{SiN}_x$  and  $\text{SiO}_2$  a dependence of the effective lifetimes and the injection depth has been observed. The effective lifetimes decrease at high injection levels for thick c-Si because the recombination is dominated in the bulk. Some decrease in lifetimes at lower injection levels has been explained to be related to bulk recombination in the depletion region (when the surface is shielded from electrons) [17].

### 1.3.3 Alumina + annealing

Hoex *et al.* (2008) reported that ALD deposited alumina as passivation performed similarly as high-temperature thermal  $\text{SiO}_2$  on lightly n-doped c-Si. This means that the negative fixed charge provided by alumina shields the surface efficiently for lightly n-doped Si, too, and should passivate the surface of c-Si [17]. Alumina provides as well good chemical passivation due to low interface defect density when deposited on c-Si [19]. Further, Hoex *et al.* (2008) studied the lifetimes in c-Si by adding positive corona charges on the surface of the alumina in order to compensate the negative fixed charges in the passivation layer. The lifetimes in c-Si showed to decrease very fast with increasing corona charge density at the surface (hence cancelling out the field-effect passivation effect). By identifying the point of minimal lifetimes, the negative fixed charge density ( $Q_f$ ) in an 26 nm  $\text{Al}_2\text{O}_3$  layer was estimated to be  $1.3 \cdot 10^{13} \text{ cm}^{-2}$ . Additionally, they found that the recombination rate is proportional to  $1/Q_f^2$  for lightly doped c-Si, independent of the positive or negative fixed charge density and could deduce that the tested 26 nm  $\text{Al}_2\text{O}_3$  layer is 2 and 4 orders of magnitude more efficient than a standard  $a\text{-SiN}_x\text{:H}$  ( $Q_f = 10^{12} \text{ cm}^{-2}$ ) and thermal  $\text{SiO}_2$  ( $Q_f = 10^{12} \text{ cm}^{-2}$ ) layer, respectively [17].

The passivation efficiency depends strongly on the injection level. Apart from the decrease in effective lifetimes at high injection levels, they decrease as well slightly at low levels. This is explained by bulk recombination losses in the shielded (electron depleted) close to the Si surface. Nevertheless, effective lifetimes exceeding 18 ms have been measured by QSSPL for flat lightly n-doped low-resistivity c-Si wafers passivated by 30 nm  $\text{Al}_2\text{O}_3$  [17]. A standard RCA1 and RCA 2 clean and a dip into diluted 1% HF prior to deposition is commonly done in order to leaving behind a H-terminated, hydrophobic c-Si surface [17, 19].

The influence of annealing on the surface passivation properties of  $\text{Al}_2\text{O}_3$  was extensively reported by Kersten *et al.* (2013). The interface trap density was affected by both, the annealing temperature and atmosphere. The fixed charge density on the contrary was influenced solemnly by the annealing temperature [19]. The best results were reported for low injection level c-Si at an annealing temperature of 470 °C,  $\text{O}_2$  atmosphere and 10 min. Temperatures above 400 °C yielded very good results for high injection levels [19]. Hoex *et al.* (2008) did an annealing process at 425 °C for 30 min in  $\text{N}_2$  atmosphere.

### 1.3.4 Titanium Dioxide

Interesting c-Si passivation results have been reported using  $\text{TiO}_2$ . Ho *et al.* (2015) reported the improvement of the conversion efficiency of c-Si thin-solar cell with a nanotextured surface from 8.13 to 9.62% after the passivation with 15 nm of  $\text{TiO}_2$  and 10 min annealing at  $300^\circ\text{C}$  in  $\text{N}_2$  atmosphere. The Si absorber thickness was about  $5.87\text{ }\mu\text{m}$  and a texture depth of 400 nm. They report a effective reduction of surface recombination after the passivation [16]. This effect is among other thanks to its appropriate band offset when in contact with c-Si, namely a small conduction, and large valence band off-set [24]. A interfacial  $\text{SiO}_2$  layer and Si-O-Ti bonds have been identified as the main chemical passivation effects [24]. Effective minority carrier lifetimes of up to 500  $\mu\text{s}$  or even 1500  $\mu\text{s}$  have been reported for low resistivity n-c-FZ-Si with only a couple of nm's of oxide. Layers thicker than 6 nm have shown to have the adversary effect due to stress-related phase transitions within the oxide layer. A common way of deposition is by ALD [24].

### 1.3.5 Combinations: multi-layer passivation

Tan *et al.* (2017) reported a very efficient double-layer passivation on pyramidal  $20\text{ }\mu\text{m}$  thin-Si with a feature size of 3-10  $\mu\text{m}$ , using a combination of  $\text{Al}_2\text{O}_3$  and  $\text{SiN}_x$ . They contrast single-layer passivation consisting of 80 nm PECVD deposited  $\text{SiN}_x$  to double-layer passivation of 3 nm ALD deposited  $\text{Al}_2\text{O}_3$  followed by 80 nm of PECVD deposited  $\text{SiN}_x$ . Comparing planar to textured Si solar cells passivated with  $\text{SiN}_x$  only, the efficiency increases by 4.5% to 15.1% for textured one. By adding the second passivation layer, the efficiency was further increased by 1.3 %, improving both the short-circuit current density and the open-circuit voltage [39].

Schmidt *et al.* (2008) compared passivation with  $\text{SiO}_2$ ,  $\text{Al}_2\text{O}_3$  and a combination of both. The surface recombination velocities of 130 nm of  $\text{Al}_2\text{O}_3$  and a stack of  $\text{Al}_2\text{O}_3/\text{SiO}_2$  30/200 nm were comparable and even inferior to annealed  $\text{SiO}_2$  [36]. This is attributed to the hydrogenation of the interface states during the silicon oxide deposition [36].

Mallorquí *et al.* (2015) compared the before mentioned approaches on pn-junction nanowire array c-Si solar cells. Similar  $V_{oc}$  and  $J_{sc}$  have been achieved for  $\text{SiN}_x$  and  $\text{Al}_2\text{O}_3$  passivated devices, resulting in efficiencies of 3.4% and 2.4%, respectively. Surprisingly, the thermally grown  $\text{SiO}_2$  that is known for high chemical passivation and good surface recombination reduction, performed very poorly with a efficiency of only 1.2 %. When a 19 nm layer of  $\text{SiN}_x$  was deposited on top of the  $\text{SiO}_2$ , the properties were greatly enhanced to an efficiency of 9.9% [25].

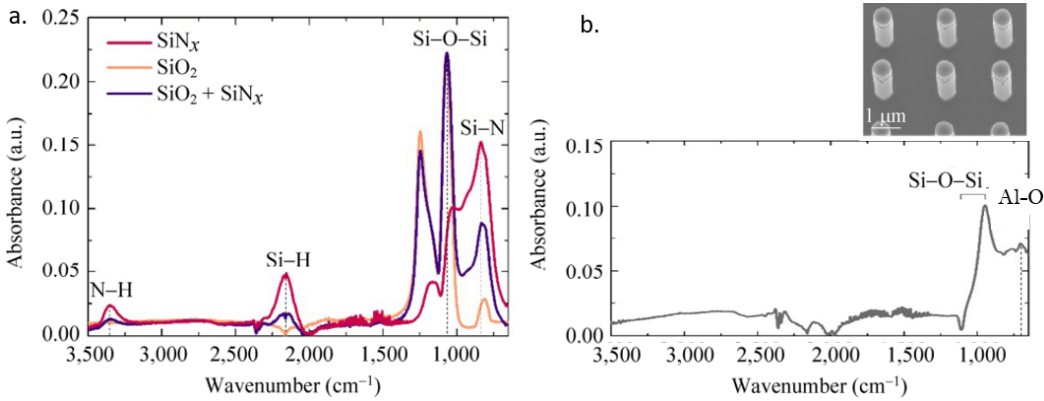
The excellent chemical passivation properties of  $\text{SiO}_2$  have been reported to further be enhanced by depositing a thin layer of Al and annealing prior to the oxide deposition. This adds positive fixed charges at the surface, providing a field-effect passivation by

keeping holes away from the surface [17]. The best surface passivation should thus be achieved for high fixed charge density and low interface trap density.

Mallorquí *et al.* (2015) investigated the interface between silicon and its passivation layer. Their results are shown in Figure 1.5. The peak denoted as Si-H for the  $\text{SiN}_x$  passivating layer was separated into six peaks representing: (1) H-Si-Si<sub>3</sub>, (2) H-Si-HSi<sub>2</sub>, (3) H-Si-NSi<sub>2</sub>, (4) H-Si-SiN<sub>2</sub>/H-Si-SiNH, (5) H-Si-HN<sub>2</sub> and (6) H-Si-N<sub>3</sub>. N-H bonds are related to the formation of trivalent silicon ( $\cdot\text{Si}\equiv\text{Si}_3$ ) dangling bonds which results in a fixed positive charge density [25].

The high chemical passivation is related to the low interface defect density. The only major defect in the Si/SiO<sub>3</sub> interface is the Si atom with a dangling bond due to a lattice mismatch and leads to a fixed positive charge. A hydrogen treatment is usually done for its passivation [25]. In the double layer appears hence the Si-H peak, being the hydrogen passivated dangling Si bond. Furthermore, the SiO<sub>2</sub> interlayer removes significantly Si-N bonds. Consequently the field-effect passivation contribution by the SiO<sub>2</sub>/SiN<sub>x</sub> double-layer is reduced [25].

As for Al<sub>2</sub>O<sub>3</sub>, apart from the Al-O peak, there's the broad Si-O-Si signal due to a thin interlayer of SiO<sub>x</sub> formed before ALD [17]. This interlayer could be beneficial by adding a high density of Al vacancies, which can, like interstitial oxygen, be charged negatively and resulting in fixed negative charges [25].



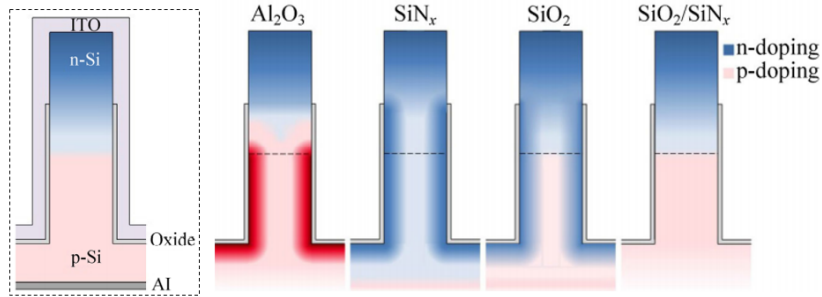
**Figure 1.5:** FTIR spectra of the interfaces between passivation layers and silicon in a nanowire array. a) Si/SiN<sub>x</sub>, Si/SiO<sub>x</sub>, Si/SiO<sub>x</sub>+SiN<sub>x</sub>. b) Si/Al<sub>2</sub>O<sub>3</sub> adapted from Mallorquí *et al.* (2015) [25].

### 1.3.6 Passivation and solar cell performance

Whereas low surface recombination velocities and high minority carrier lifetimes are good indicators for efficient charge generation and dynamics at the surface, they do not imply better solar cell performance [25]. This might become particularly true for nanopatterned

solar cells, as observed by Mallorquí *et al.* (2015) for arrays of nanowires (NWs). The above mentioned oddity of  $\text{SiO}_2$  leading to a good chemical passivation, nevertheless performing badly in solar conversion, is related to the high aspect ratios of the structure. In the case of a positive fixed charge, electrons are attracted towards the surface and holes are forced towards the core of the NW. In low p-doped regions of the Si NWs, holes become minority carriers and the pn-junction is moved to the base of the NWs for high positive fixed charge densities. This is illustrated in Figure 1.6. For low positive fixed charges, no inversion happens in flat Si. In NWs however, inversion can occur directly at the surface, leading to an annihilation of hole and electron densities somewhere in the core. In this region of similar densities, significant recombination occurs and the properties degrade [25]. Generally, inversion occurs when the charge in the passivating layer is higher than what the ionized dopants in the depletion layer can balance [9]. For Si/ $\text{SiN}_x$  the junction is pushed to the base of the NWs, decreasing the surface recombination. With Si/ $\text{Al}_2\text{O}_3$  passivation inversion occurs in the NWs due to the very specific pn-junction position of their architecture.

In conclusion, when using high aspect ratio structures, the passivation can result in opposite results due to the small dimensions, as the depletion layers might come close to the feature size.



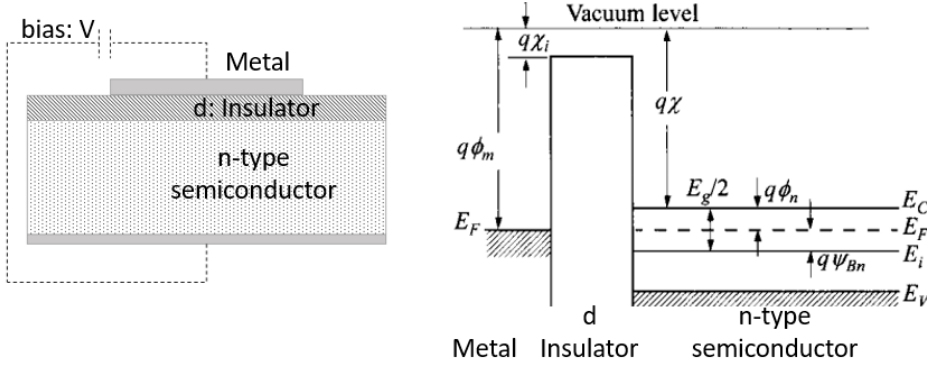
**Figure 1.6:** Illustration of the carrier density profile in the NW of a solar cell based on high aspect ratio NW arrays by Mallorquí *et al.* (2015). Depending on the passivation materials, the pn-junction (dashed line: initial position) is moved and inversion regions with increased recombination might occur [25].

## 1.4 Characterization of thin silicon

### 1.4.1 Capacitance methods: MOS devices

The surface physics of silicon can be studied by means of metal-oxide-silicon (MOS) structures, as shown in Figure 1.7, left. This method gives access to the capacitance of the layers which are a good mean to characterize the semiconductor/oxide interface trap

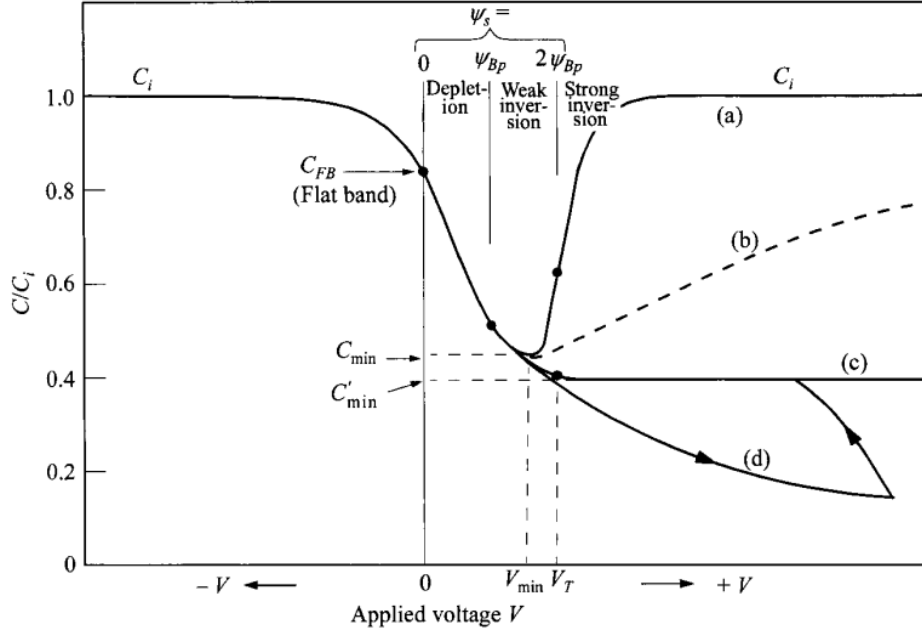
density distribution [28]. One quantification approach of the interface trap density is based on the comparison of the ideal C-V graph with the measured C-V curves (i.e. *non ideal*). This is called the Terman method, using the full interface state method [28, 31, 38, 41].



**Figure 1.7:** Scheme of a typical metal-insulator-semiconductor (MIS) capacitor (left) with energy band diagram without applied bias at equilibrium ( $V=0$ ) (right). *Courtesy of Sze et al. [38].*

As can be seen on Figure 1.7, left, the contacting of the surface is necessary and is done by metallic contacts (solid-state contacts) on flat MOS systems. However, on high aspect ratio structures this is very tedious and imprecise which makes many characterization methods unsuitable for nanostructured materials. The use of electrochemical impedance spectroscopy (EIS) to obtain the interface trap densities has been used widely for such materials. This method replaces the solid-state contacts with a highly conductive electrolyte, which makes conformal electrical contact [27, 28]. The capacitance of the MOS device changes depending on the applied DC voltage and is frequency dependent, as shown in Figure 1.8. The electrolyte of high ion concentration blocks efficiently the semiconductor.

**Basic relations** As illustrated in Figure 1.9, under applied bias, three regimes can be distinguished at a n-type semiconductor surface. (i) *accumulation* for  $V>0$ : close to the surface the conduction-band edge  $E_C$  bends downward, approaching the Fermi level and as the carrier density depends exponentially on  $\Delta E = E_C - E_F$ , electrons accumulate locally. (ii) *depletion* for  $V<0$ : the bands bend upward under depletion of the majority carriers. (iii) *inversion* under  $V\ll 0$ : the bands bend stronger. As the intrinsic level crosses over the Fermi level, locally the number of minority (holes) is larger than the number of majority charge carriers. As an ideal MOS structure is considered, no Fermi-level bending occurs and no current flows and  $dE_F/dx = 0$ . When the DC voltage is swept with a certain frequency, then the semiconductor undergoes inversion, depletion, and accumulation



**Figure 1.8:** C-V curve of a MOS structure undergoing inversion, depletion and accumulation for a) low frequency (quasistatic), b) intermediate frequency, c) high frequency [38].

with increasing voltage (versus reference electrode), as shown in Figure 1.8. For the low frequency case, the capacitance increases anew as a thin inversion layer forms at the interface [28, 38].

The semiconductor surface potential is defined as  $\Psi_S \equiv \Psi_n(x \rightarrow 0)$  with respect to the bulk ( $x = \infty$ ) with:

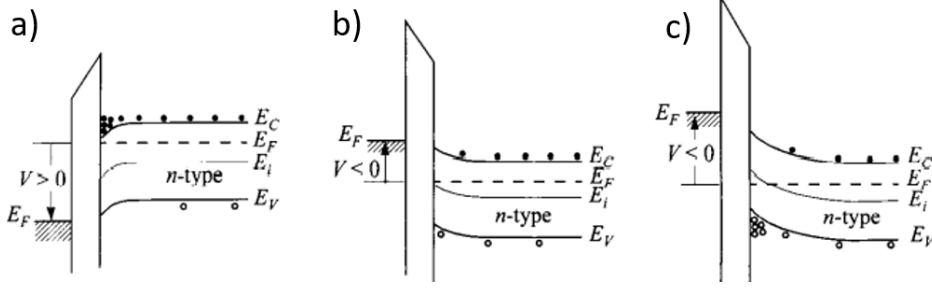
$$\Psi_n(x) \equiv \frac{E_i(x) - E_i(\infty)}{q} \quad (1.4)$$

The Fermi-level is in flat-band condition, if  $V = 0$  where  $\Psi_S = 0$ . Depletion occurs when  $\Psi_S \in [\Psi_{Bn}, 0]$ , weak inversion when  $\Psi_S = \Psi_{Bn}$  and strong inversion when  $\Psi_S = 2\Psi_{Bn}$ .

If  $C_D$  is the semiconductor depletion layer capacitance, then the total capacitance can be expressed as the two in series:

$$C = \frac{C_i C_D}{C_i + C_D} \quad (1.5)$$

Where  $C_i$  is constant for a certain thickness,  $C_D$  depends both on the net charge distribution on the semiconductor surface, i.e the surface voltage  $\Psi_S$  and voltage drop, and the measurement frequency. It can be expressed as  $C_D \equiv dQ_S/d\Psi_S$  (differentiating the excess surface charge with respect to the surface potential) [38, 41]. The capacitance and the



**Figure 1.9:** Band diagram for ideal MIS capacitors with a n-type semiconductor in different regimes: a) accumulation for  $V > 0$ , b) depletion for  $V < 0$ , c) inversion for  $V \ll 0$  [38].

density of interface traps are related as [31]:

$$C_{it} \equiv \frac{dQ_{it}}{d\psi_s} = q^2 D_{it} \quad (1.6)$$

As the voltage increases, both, the depletion width  $W_D$  and the surface potential  $\psi_s$ , increase. The depletion width reaches a maximum when the strong inversion regime is reached at  $\psi_s = 2\psi_{Bn}$  [31].

**Electrolyte-semiconductor surface dynamics** When an electrolyte is in contact with a semiconductor, the redox potential in the electrolyte and the Fermi energy in the semiconductor align via band bending. For an n-type semiconductor with  $E_F > E_{redox}$ , electrons are released from the semiconductor to the solution. The electron depleted region of the semiconductor is called space charge (SC) layer within which the bands are bent upwards to equilibrium with the increased  $E_{redox}$ . In the electrolyte this charged region is denoted the Helmholtz layer [45].

Energy states closest to the surface are able to transfer charges between the electrolyte and the semiconductor. If a voltage is applied, then all the layers contribute:  $\Delta V = \Delta V_{SC} + \Delta V_H$  and the neutrality among exchanged charges requires:  $Q_{solution} = Q_{SC} + Q_{SS}$ . The total capacitance of the interface can be expressed as:

$$\frac{1}{C_{tot}} = \frac{1}{C_{sc} + C_{ss}} + \frac{1}{C_H} \quad (1.7)$$

As applied by Meng (2017) and Mikulik (2018) *et al.*, the circuit of a MOS capacitor with a electrolyte replacing the metal gate simplifies to the solid-state case. The electrical double layer capacitance is typically 10x greater than the oxide capacitance in these setups and can be ignored [27, 28].

Hence, when looking at the dynamics between applied voltage and measured capacitance, information about the surface states (SS) can be extracted. For a semiconductor

with a low density of surface states ( $C_H \gg C_{SC}$ ) and with  $E_{redox} \sim E_F$  (i.e.  $C_{SS} \ll C_{SC}$ ), the Mott-Schottky equation is derived, relating the interface capacitance to the electrode potential [14, 44, 45]:

$$\frac{1}{C_{sc}^2} = \frac{2}{e\epsilon\epsilon_0 N_d} \cdot \left( (V_{applied} - V_{fb}) - \frac{k_B T}{e} \right) \quad (1.8)$$

By plotting  $1/C_{sc}^2$  vs.  $V$  and fitting a line to the linear part of the graph, the flat band potential can be extracted at its intersection with the V-axis and the slope gives the doping level  $N_d$  [12, 45]. The slope of the plateau is closely correlated to the density of surface states. The bigger the slope, the fewer surface states and the smaller the depletion region, and vice versa [45]. Hence this slope can be used for qualitative comparison of interface trap states between among different.

### 1.4.2 Photoluminescence

With photoluminescence the near bandgap recombination radiation (*photoluminescence*) after photoexcitation is measured. The band-to-band PL signal gives fundamental information about the absorption coefficient, radiative recombination coefficient and the influence doping of the bandgap. Applied to photovoltaics, parameters like the diffusion length of minority carriers can be extracted or the light trapping efficiency of plasmonic structures can be evaluated [30]. Time-resolved (TRPL) or quasi-steady-state (QSSPL) photoluminescence are both non-destructive and very sensitive techniques, adapted to small and thin samples with the detection potential of low emission signals. In TRPL the excess minority-carrier concentration can be measured as a function of time and gives access to the transient decay of the photoluminescence signal, correlated to the minority-carrier density. The latter is dependent on both, the carrier lifetime and the diffusion rate and is thus structure dependent [2]. In QSSPL the radiative recombination of continuously generated excess charge carriers is measured.

For bulk silicon, the effective lifetime can be written as [2]:

$$\frac{1}{\tau_{PL}} = \frac{1}{\tau_B} + \frac{2S}{d} \quad (1.9)$$

With  $S$  the interface recombination velocity,  $d$  the active layer thickness and  $\tau_B$  the bulk lifetime.

## 2.1 Fabrication of HUD thin silicon solar cells

The goal is to find a perfect passivation recipe on low n-doped CZ (001)-silicon wafers and to reproduce it on thinned-down solar cells. First, the effects of HUD nanostructures was to be studied on thick 500  $\mu\text{m}$  silicon. Then passivation layers of amorphous  $\text{Al}_2\text{O}_3$ , amorphous  $\text{SiO}_2$ , amorphous  $\text{Si}_2\text{N}_3$  and combinations thereof were to be tested on these thick Si samples. The same recipes were to be then tested on diverse thin nanostructured silicon samples. Finally, the most promising procedures were to be repeated on thinned-down silicon solar cells. The materials used are 10  $\mu\text{m}$  (University Wafer), 20  $\mu\text{m}$  (provider not specified), 30  $\mu\text{m}$  (Virginia Wafers) and 500  $\mu\text{m}$  (Seifert Albert) moderately n-doped ( $10^{15}\text{cm}^{-3}$  CZ dsp (001)-silicon wafers and finally, approximately 50  $\mu\text{m}$  thin IBC Si-solar cells. Whereas the 10 and 30  $\mu\text{m}$  Si wafers were free-standing wafers of 1" diameter and needed to be bonded onto quartz substrates, the 20  $\mu\text{m}$  Si wafers were already bonded by PMMA onto 1 mm Si. As the backside of the thinned-down solar cells are protected by parylene, processing temperatures shouldn't exceed the degradation temperature of 250°C.

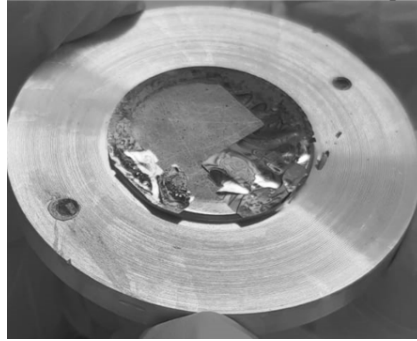
### 2.1.1 Bonding and debonding of thin-Si wafers

During the handling of the thin-Si wafers, air flow needs to be taken into account. It is sufficient to make the wafers levitate and crash or bond statically somewhere. When the wafers are bonded only with water to the substrate, the static attraction to the wafer box was enough to lift the wafers from the substrate. To impede this, a piece of lens paper (Salm en Kipp BV) was used as a protection.

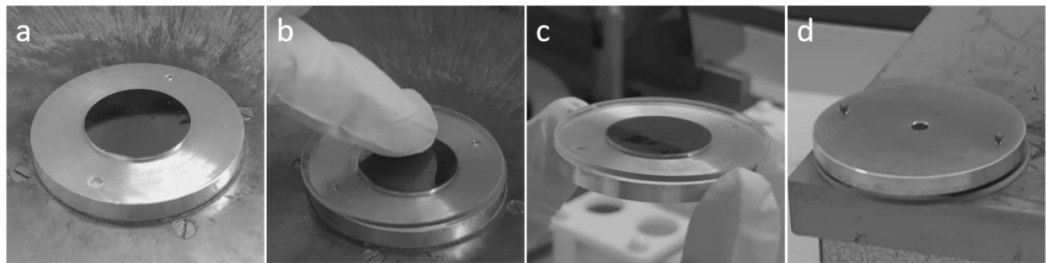
**1" thin-Si wafers** The 10 and 30  $\mu\text{m}$  silicon wafers are very fragile and they were bonded to a substrate before imprint. The mount of the spin-coater needs to be of perfect surface quality in order to reduce the risks of breakage. If PMMA flows between the holder and the wafer during the spin-coating, due to edge cracks for example, then the wafers are most likely to break upon removal of the holder and could stay sticking partially to the holder (Figure 2.1).

A 2" 1.5 mm thick quartz wafer was used as a carrier wafer. The procedure is shown in Figure 2.2. The Si wafer was hold by vacuum suction while 400 nm PMMA were

spin-coated on top. The carrier wafer was positioned gently and pressed lightly on the Si wafer. The whole stack is then transferred to a hot plate and cured at 120°C for 4 minutes. The difference in thermal expansion between both materials didn't induce any cracking and eventually even aided the detachment. The vacuum that held the carrier wafer to the mount should release automatically after maximally a couple of minutes. Alternatively, pressured nitrogen could be applied through the backside of the holder.



**Figure 2.1:** Incomplete debonding of a 30  $\mu\text{m}$  silicon wafer after an attempt to bond it to a carrier quartz wafer.



**Figure 2.2:** Bonding procedure for thin-Si wafers. a) Vacuum-bonded 30  $\mu\text{m}$  Si wafer on a customized mount. b) Bonding to a 1.5 mm thick quartz wafer after spin-coating of 400 nm PMMA. c) Transfer of the whole stack. d) Curing of the stack up-side down at 120°C for 4 minutes. The vacuum seal should release after a couple of minutes and the Si wafer remains bonded to the quartz.

Successively, in order to debond the wafer from the quartz, it was left to sit in an acetone bath for a couple of hours. Afterwards, by sliding it several times into water at a 45° angle with respect to the surface, it should float up onto the water surface at once.

**20  $\mu\text{m}$  thin-Si wafers** As the 20  $\mu\text{m}$  were already bonded by PMMA to 1 mm Si, the full stack could be cleaved in custom sized pieces. To do so, the wafers were nudged deeply thin-Si on top. This yielded better edge quality than having the thin-Si on the

bottom. Micro cracks were easily induced at the edges, making the wafer more prone to breakage or loosing small debris. The samples were imprinted in the bonded state. For debonding, an acetone bath was used again. However, as the substrate (thick Si) didn't have any excess area under the thin-Si, it couldn't be grabbed with a pair of tweezers and repetitively immersed in water until flotation. Hence, the debonding was done manually immersed in water. The sample spent 24h upside-up in an acetone bath, dissolving the PMMA. Then, the thin wafer was guided gently with a pair of tweezers onto the immersed future substrate. The latter could afterwards be lifted and as the water evaporated, the 20  $\mu\text{m}$  wafer remained bonded. A faster method is debonding by thermal expansion. Some of bonded samples have as well been passivated directly in order to see if the conformally deposited oxide would hinder the debonding by acetone. This showed that by putting the stack on a 250 °C hotplate didn't induce any cracks but smoothly debonded the thin-Si within a couple of seconds instead. This however doesn't dissolve and remove the residual PMMA.

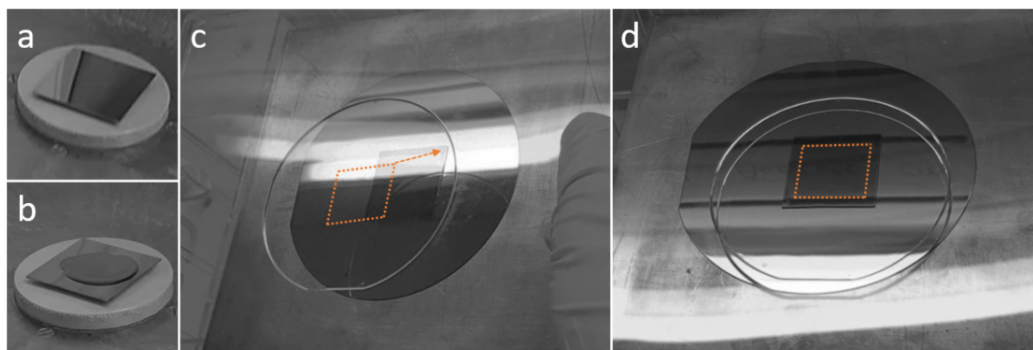
### 2.1.2 Imprinting: SCIL

The method presented has been developed under tedious analysis and step-by-step adaptation of the process by a previous group member. The final SCIL procedure is shown in Figure 2.3. First, 250 nm solgel are spin-coated on the vacuum held sample. Then it was transferred to a support that would allow free gliding (fixed and polished 4" Si wafer). The stamp was placed carefully, well-oriented on the sample and pressure was applied with a rolling motion of the thumb. After 9 minutes of evaporation time, the stack was turned upside-down and the stamp was bent slightly until all the edges were detached. The sample was removed at once with a pair of tweezers. The stamp was rinsed after each use consecutively with water-ethanol-water and nitrogen dried. If small debris remained stuck to the stamp, another mock stamping cycle can be done to remove it.

The stamped sample underwent three etching steps, using the Oxford 100 Cobra system. First, the solgel and the PMMA were etched with a 120 s  $\text{CHF}_3$  step at 20°C, preceded by a  $\text{O}_2$  plasma clean. Afterwards, the system was heated up to 60°C and the native oxide was etched with a  $\text{Cl}_2$  step. Finally, the silicon was etched with  $\text{HBr}/\text{O}_2$ . The etch time directly determines the depth of the final structure. 40 s of etch time aims roughly for 250 nm depth of the spinodal structure.

Last but not least, the solgel and PMMA were removed with an 1% HF dip for 90 s and the final HUD structure was revealed. Initially, the lift off was supposed to be easily done by a heated acetone bath. However, this didn't work. Probably, the structure is too small and the acetone cannot penetrate the trenches. Hence the more toxic and time consuming method was chosen for this work.

The samples didn't undergo any additional cleaning steps and the wafers were used as-clean from the box. Base-pirana for instance modified the surface and different etching



**Figure 2.3:** Manual SCIL printing procedure. a) Vacuum-bonded 500  $\mu\text{m}$  Si wafer on sample holder. b) Spin-coating of 200 nm Solgel on the silicon sample. c) Orientation of the stamp. d) Lowering of the stamp. Pressure is applied manually with a rolling motion of the thumb. After 9 minutes of evaporation time, the stamp can be removed.

results have been observed. The trade-off between perfect reproducibility from thick to thin Si wafers and the risk of breakage of thin-Si due to additional steps needed to be found.

## 2.2 Passivation Techniques

### 2.2.1 Deposition of amorphous $\text{Al}_2\text{O}_3$ and annealing

After the 1% HF dip, the samples were stored for several days in the clean room. No additional treatment or cleaning procedure was done prior to alumina deposition.

$\text{Al}_2\text{O}_3$  was deposited by a home-built atomic-layer deposition system (ALD). The deposition of alumina occurs atomic layer by atomic layer in alternating self-limited surface reactions. The chamber is filled successively with precursors, that react with the surface till saturation. Each flush consists of a half-reaction. The deposition rate is 0.125 nm per minute and is conformal even on high aspect ratio 3D structures [17]. The samples were positioned on a hot plate at 250°C in the center of the chamber. The precursor used was trimethylaluminium ( $\text{Al}(\text{CH}_3)_3$ , Sigma-Aldrich). One cycle consisted of a 20 ms vapor pulse of  $\text{Al}(\text{CH}_3)_3$ , followed by a delay of 18 s, a pulse of 20 ms of water (MiliQ), another delay of 18 s, before starting over again. The base pressure of the chamber was kept at 1.1 mbar, controlled by an influx of  $\text{N}_2$  with respect to the vacuum pump. At these temperatures the hydrogen content is 1-2%at [17].

The samples were annealed on a hot plate in air at 420°C for 10 min. The 20  $\mu\text{m}$  samples were annealed loose without any carrier wafer. On the one hand, the glass carrier wafer would have cracked at such high temperature and risked to break the thin-Si, on the other, the PMMA and water bonds did not sustain the 250°C of the ALD and the thin-Si started

to levitate. After annealing they were again bonded either by water or PMMA to a carrier wafer.

### 2.2.2 Deposition of amorphous SiO<sub>2</sub>

Amorphous SiO<sub>2</sub> was deposited by plasmonically enhanced chemical vapor deposition (PECVD). The recipe consists of six steps. The main steps are an oxygen plasma clean (30 s at 150°C) to remove water and organic material from the sample surface, striking the plasma (10 s at 150°C) and finally the deposition of a-SiO<sub>2</sub> at 150°C (SiH<sub>4</sub> and N<sub>2</sub>O gas flow of 4.9 and 13.1 sccm, respectively), yielding a deposition rate of 14-15 nm per minute. The refractive index has been reported to follow literature values.

### 2.2.3 Deposition of SiN<sub>x</sub>

SiN<sub>x</sub> was deposited by plasmonically enhanced chemical vapor deposition (PECVD). The recipe is very similar to the one used for a-SiO<sub>2</sub>. The temperature of the chamber was kept at 100°C throughout the whole process and the SiH<sub>4</sub> and N<sub>2</sub>O gas flow were kept at 15.0 and 14.2 sccm, respectively. The growth rate is 16-17 nm per minute. The composition of the silicon nitride is Si<sub>3</sub>N<sub>4</sub> for a layer thickness of 250 nm. The refractive index is about 2.5% lower than literature values with an increasing deviation for thinner layers. An average value of  $n_{\text{Si}_3\text{N}_4} = 2$  is taken.

The finally produced samples are listed in Table 2.1.

Si [ $\mu\text{m}$ ]	texture	passivation	layer [nm]	method
500 & 20	flat & spinodal	native	-	-
500	flat & spinodal	SiO <sub>2</sub>	5	PECVD
500 & 20	flat & spinodal	SiO <sub>2</sub>	10	PECVD
500	flat & spinodal	Al <sub>2</sub> O <sub>3</sub>	5	ALD
500 & 20	flat & spinodal	Al <sub>2</sub> O <sub>3</sub>	10	ALD
500 & 20	flat & spinodal	Al <sub>2</sub> O <sub>3</sub> + anneal	10	ALD + hotplate
500 & 20	flat & spinodal	Al <sub>2</sub> O <sub>3</sub> + anneal	10	ALD + hotplate
		+ Si <sub>3</sub> N <sub>4</sub>	+ 250	+ PECVD
500 & 20	flat & spinodal	Si <sub>3</sub> N <sub>4</sub>	250	PECVD
500	flat	TiO <sub>2</sub>	10	ALD

**Table 2.1:** Overview of the final passivation schemes. All samples have native oxide between the passivation layer and the silicon.



### 3.1 Evaluation of optical properties with UV-VIS spectroscopy

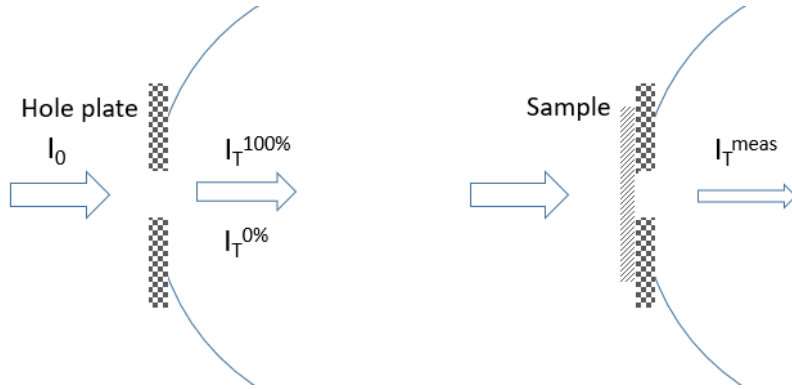
The UV-VIS setup used is a Perkin Elmer LAMBDA 750 UV/VIS/NIR spectrophotometer. The light source is a tungsten halogen lamp. High measurement stability is provided through a double-beam, double-monochromator design [33]. A switch in monochromators occurs at 860 nm, introducing some fluctuation in the collected data.

Two options are available to measure the absorption of a sample. First, the absorption is measured directly by hanging the sample in the center of the integrating sphere. Whereas this approach is very straight forward and accurate, a major drawback is poor beam incidence area control on the sample. If only the front side or certain areas of the sample want to be measured, the remaining of the sample needs to be covered.

In order to control the area exposed to the beam, the absorption can be calculated from separate transmission and reflection measurements by placing the sample at the front or back of the integrating sphere, respectively. Automatic baseline correction is available, however the baseline measurements need to be defined differently.

#### 3.1.1 Transmission measurement

In transmission mode, the sample was placed where the beam enters the integrating sphere. An aluminium plate with a 6 mm hole was used to restrict the area of the sample exposed to the beam. The side of the plate facing the integrating sphere was whitened with a highly dispersive paint (labsphere 6080, theoretical reflective spectrum in Annex Figure 6.2), whereas the other in contact with the sample was covered with a non-conductive polymeric black paint. An iris was placed at the focal point of the beam in order to limit the beam diameter to fit the hole size. The baseline for 100% transmission ( $I_T^{100\%}$ ) is solely the hole plate, as shown in Figure 3.1, left. 0% transmission ( $I_T^{0\%}$ ) is measured by blocking the sample beam. During the measurement, the beam hits the sample and a share of the transmitted light enters the integrating sphere through the hole. As the hole is aligned with the iris-reduced beam and no important in-plane dispersion in the sample is assumed, most of the transmitted light reaches the integrating sphere.



**Figure 3.1:** UV-VIS transmittance measurement scheme with baseline correction and beam area exposure control with an aluminium hole plate. Left: Open hole corresponding to 100% transmittance baseline measurement. Right: Sample measurement configuration.

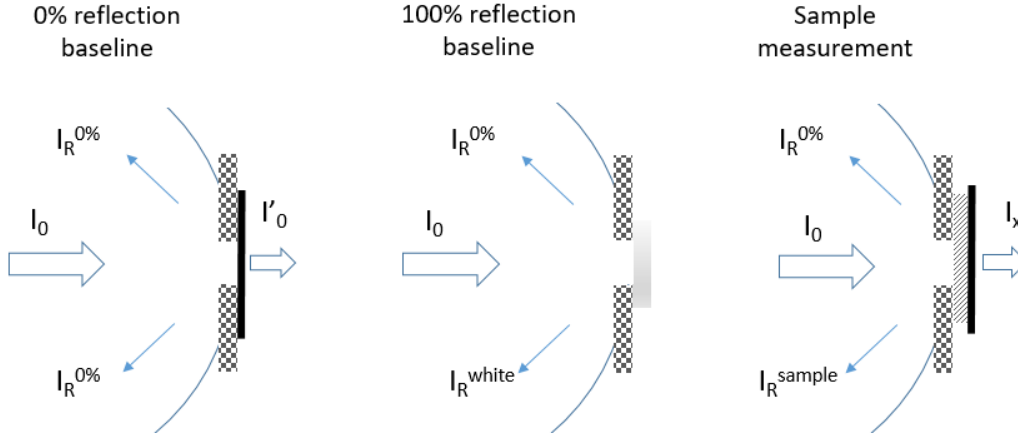
Analytically this can be expressed as:

$$T^{sample} = \frac{I_T^{meas} - I_T^{0\%}}{I_T^{100\%} - I_T^{0\%}} = \frac{I_T^{sample}}{I_0} \quad (3.1)$$

Where  $I_T^{sample}$  corresponds to the true intensity transmitted by the sample after subtracting any background light and  $I_0$  the maximal light intensity reaching the integrating sphere.

### 3.1.2 Reflection measurement

In reflection mode, the sample was placed at the back of the integrating sphere at a small constant angle with respect to the source. The hole plate was again placed accordingly to the beam, the whitened face facing the integrating sphere. The baseline for 100% reflection ( $I_R^{100\%}$ ) was measured using a silver mirror (Thorlabs PF10-03-P01), shown in Figure 3.2, center. The provider indicates a spectral reflectance of about 97%. Initially, 100% reflection was measured using a piece of the same material the sphere is made from. However, when measuring the reflection of the mirror with respect to the white piece, it proved 10% more reflective and was therefore chosen as the reference. The holder of the mirror introduced a 1 mm gap between the hole plate and the mirror surface. 0% reflection would ideally be measured by open space (open hole, mimicking a black body), or, as suggested by the provider, using a blackened hood over the sample. However, when measuring a black tape with respect to the open space, a reflection of -100% was obtained. Therefore, a thick layer of tape was used as 0% reflection ( $I_R^{0\%}$ ) (Figure 3.2, left). When measuring the sample, the same black tape is placed directly behind. Without tape the measured reflectance was



**Figure 3.2:** UV-VIS reflectance measurement scheme with baseline correction and beam area exposure control with an aluminium hole plate. Left: black tape for 0% reflectance baseline measurement. Center: Silver mirror for 100% reflectance. Right: Sample measurement configuration, where black tape is placed behind the sample.

overestimated for very thin samples. The final configuration is shown in Figure 3.2, right.

Considering that 100% reflection is the sum of whatever is reflected by the open integrating sphere ( $I_R^{0\%}$ ) and the reflection of the mirror:  $I_R^{100\%} = I_R^{mirror} + I_R^{0\%}$ , and the measured intensity is the sum of the open integrating sphere and the sample:  $I_R^{meas} = I_R^{0\%} + I_R^{sample}$ , then the relative measured reflectance is:

$$R^{meas} = \frac{I_R^{meas} - I_R^{0\%}}{I_R^{100\%} - I_R^{0\%}} = \frac{I_R^{sample}}{I_R^{mirror} + I_R^{0\%} - I_R^{0\%}} = \frac{I_R^{sample}}{I_R^{mirror}} = \frac{I_R^{sample}}{\alpha_\lambda \cdot I_0} \quad (3.2)$$

Where  $\alpha_\lambda$  is the spectral reflectance of the mirror. The reflectance of the sample can be expressed as:  $R^{sample} = \alpha_\lambda \cdot R^{meas}$ .

### 3.1.3 Comparison with analytical results

As a comparison to the experimental data, the stack of layers was simulated by implementing the Fresnel equations for an unpolarized and perpendicular incident light beam. Three different scenarios were considered:

- Flat silicon: Si sandwiched between two semi-infinite air layers with  $n = 1$
- Patterned silicon: Si + HUD layer with 280 nm thickness and refractive index determined from equation 1.1, sandwiched between two semi-infinite air layers

- The previous two cases + a dielectric layer with the respective refractive index.

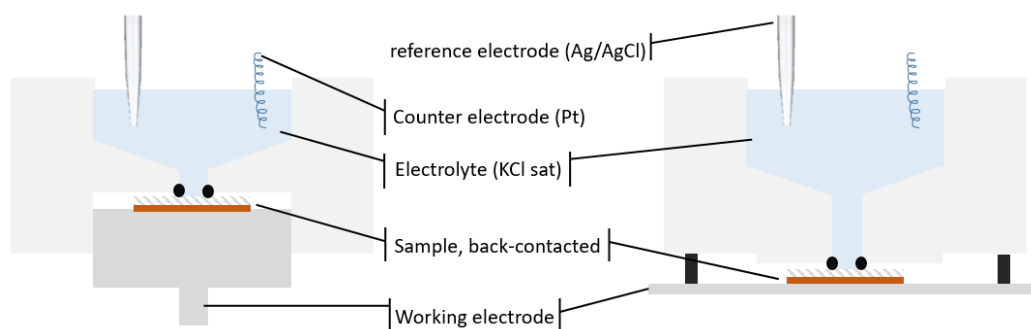
For simplification, the spectral dependence of the refractive index for the passivation layers was neglected. The filling fraction for the HUD spinodal structures were determined from SEM images without tilt, using a pixel count feature of a image processing software, as shown in the appendix, Figure 6.4.

The post-processing included a smoothing of the curves by doing an averaging over 10 points and a correction of non-perfect reflection of the silver mirror.

## 3.2 EIS and CV

### 3.2.1 Setup and measurement technique

Electrochemical impedance spectrometry (EIS) was conducted using a Potentiostat (SP-300 by BioLogic) and a customized electrochemical cell. The cell offers two ways to back-contact the samples. First, the sample can be directly contacted through a conductive holder that is used to screw the sample into the cell until in tight contact with the O-ring (Figure 3.3, left). This was ideal for 500  $\mu\text{m}$  silicon samples that wouldn't break under the minor tangential forces applied when screwed into tight contact with the O-ring. In this setup the native oxide was scratched on the backside with a diamond tip and eutectic InGa was applied for contacting. In order to improve the contact surface, a copper tape stack was used in direct contact with the InGa.



**Figure 3.3:** EIS setup using a Ag/AgCl with 3M KCl solution as reference electrode and a platinum coil as counter electrode. The electrolyte is a saturated KCl solution, in contact with the back-contacted sample connected to the working electrode. The solution is confined using a leak-proof O-ring.

Second, the sample can be pressed against the O-ring by mounting the cell vertically onto a conducting holder, as shown in Figure 3.3 (right). In this case, the forces acting upon the sample are only vertical and this configuration is thus adapted for thin-Si. A with 30 nm Al covered silicon piece was used as a substrate. The Al was deposited with an

E-beam system from Polytechnik. In contrast to the 500  $\mu\text{m}$  Si, on the thin Si the native oxide on the back side needed to be removed chemically by HF, not mechanically. In order to protect any layers deposited on the front side, a HF resist (Allresist, AZ1518 SX AR-PC 5000/40) was spin-coated before the HF dip. Afterwards, a 30 nm Al layer was deposited on the etched surface. Finally, the HF resist was removed in an acetone bath. The Al-contacted thin-Si was bonded with water onto the Al-covered substrate. The latter was sandwiched against the O-ring with four screws, tightened equally.

A three electrode scheme was used. The reference electrode used was an Ag/AgCl (3M KCl) (BASI, RE-5B) and the counter electrode a platinum coil. Both electrodes were immersed equally in a saturated KCl solution. The parameters for EIS were chosen as described by Mikulik *et al.* (2018) and Meng *et al.* (2017) [27, 28]. The frequency range for EIS was 1-100 kHz with an AC oscillation amplitude of 10 mV and 7 frequency steps. By first conducting an IV-measurement, the substrate voltage range was determined for every sample, such that no current would flow. The open-circuit potential was assessed before starting the measurement. As the equipment run into technical issues by getting stuck at random moments throughout the cyclic frequency swipes, single-frequency measurements were done afterwards.

### 3.2.2 Analysis of the data

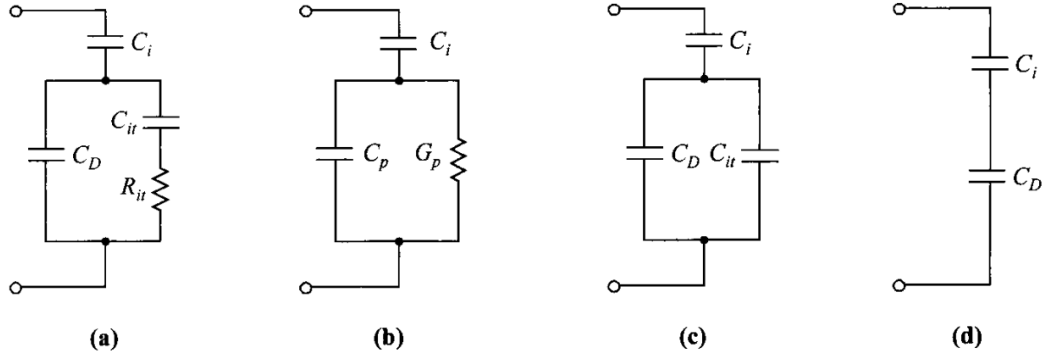
For the analysis of EIS data, different methods are being used. Essentially, they depend on the frequency range accessible by the setup. The Low-Frequency Capacitance Method uses the low-frequency equivalent circuit (Figure 3.4, c) [21, 38, 42], the High-Frequency Method uses the high-frequency equivalent circuit (Figure 3.4, d) [23, 31, 38, 41] and the High-Low-Frequency Capacitance Method is based on a combination of both [7, 32, 38]. It is often completed by conductance-voltage measurements for lifetime calculations [6, 7, 23, 27].

The EIS setup at hand has an upper limit of 200 kHz and the low frequency limit cannot be reached. Hence, the high-frequency method by Terman is to be implemented [41]. In order to understand the method, some basic relations shall be introduced here.

## 3.3 Measurement of Interface Traps in silicon using MOS capacitors: the Terman method

The system of an insulator and semiconductor described by equation 1.5 can be extended to an equivalent circuit, incorporating the influence of the interface trap states in silicon. A capacitance  $C_{it}$  and resistance  $R_{it}$  are included, both functions of energy. The interface-trap lifetime is defined as  $\tau_{it} = C_{it} \cdot R_{it}$ , describing the response of the traps to the applied

frequency. In Figure 3.4, a the representative circuit is shown.



**Figure 3.4:** Equivalent circuits describing the MOS system including interface traps.  $C_{it}$  and  $R_{it}$  are the capacitance and resistance associated with the interface traps. a)  $C_{it}$  and  $R_{it}$  in parallel with the semiconductor depletion capacitance. b) Conversion into a frequency-dependent capacitance  $C_p$  in parallel with frequency-dependent conductance  $G_p$ . c) Low-frequency limit. d) High-frequency limit [38].

In the high-frequency limit, the influence of the interface trap states can basically be ignored (Figure 3.4), as the traps cannot respond fast enough to the high frequency and the analytical expression for the high-frequency capacitance  $C_{HF}$  reduces to equation 1.5 [38]. For a certain depletion layer capacitance  $C_D$ , the high frequency capacitance of a MOS capacitor will be the same as that of an ideal capacitor without interface traps. However, besides the effect of the two additional circuit elements  $C_{it}$  and  $R_{it}$ , the interface traps affect as well indirectly  $C_D$ . They take up some of the charges, that otherwise would have been used to deplete the layer. Hence,  $C_D$  is lowered, resulting in a lower surface potential or less band bending. Therefore, the measured capacitance-voltage relation will as well be altered in the high-frequency case [31, 38]. This causes a stretch and distortion of the ideal C-V curve 3.5, left) [31].

At same band bending (surface voltage)  $\Psi_S$ ,  $C_{HF}$  will be the same as  $C_{HF}^{ideal}$ . Therefore, if  $\Psi_S$ , corresponding to a certain  $C_{HF}^{ideal}$ , can be determined, and the applied voltage  $V$  corresponding to the same  $C_{HF}$  with traps measured, the band bending  $\Psi_S$  vs.  $V$  relation can be established, as illustrated in Figure 3.5. There, all the information about the interface trap level density is contained [31].

In order to express the change of the semiconductor surface voltage  $\Psi_S$  with respect to

the density of interface traps,  $\Psi_S$  is isolated from the applied voltage using, equation 1.5:

$$\frac{d\Psi_S}{dV} = \frac{C_i}{C_i + C_D(\Psi_S) + C_{it}(\Psi_S)} \quad (3.3)$$

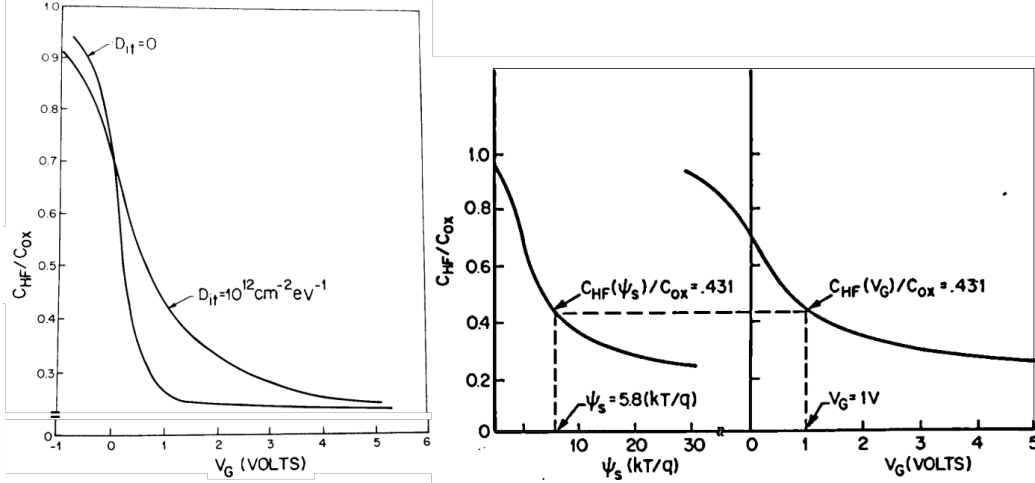
And hence:

$$C_{it}(\Psi_S) = C_D \left[ \left( \frac{d\Psi_S}{dV} \right)^{-1} - 1 \right] - C_S(\Psi_S) \quad (3.4)$$

And using equation 1.6 in 3.4,  $D_{it}$  can be determined. This results in the analytical expression:

$$D_{it} = \frac{C_i}{q^2} \left[ \left( \frac{d\Psi_S}{dV} \right)^{-1} - 1 \right] - \frac{C_D}{q^2} \quad (3.5)$$

For a certain  $C_D$ -V plot, the band bending  $\Psi_S$  for silicon can be determined from theory and equation 3.5 finally gives the interface trap state density  $D_{it}$ .



**Figure 3.5:** Left:  $C$  vs.  $V$  curve stretch due to the presence of interface trap states. Right: Illustration of the implementation of the Terman high-frequency method, determining  $\Psi_S$ - $V$  relation for the calculation of the interface trap capacitance. *Courtesy of Nicollian et al. (1982), p.328 [31].*

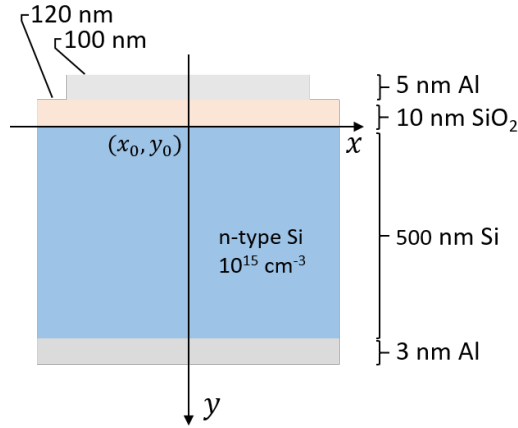
### 3.3.1 Ideal $\Psi_S$ vs. $V$ curves for the high-frequency Terman method

In order to get the capacitance vs. surface potential curves ( $C$ - $\Psi_S$ ), the NextNano software package was used [4] in order to solve the 1D Schrödinger-Poisson equations. A great tutorial is made available by the developers [10] and was adapted accordingly.

The Si/passivation layer/electrolyte MOS capacitor was approximated as a Si/passivation layer/Al MOS capacitor with a Schottky contact. For silicon with 10 nm of a-SiO<sub>2</sub> a value of  $\phi_b = 0.7$  eV was used as the Schottky barrier height [5]. The doping concentration found via the Mott-Schottky plot, equation 1.8, was used as the number of charge carriers. It was set to  $10^{15}$  cm<sup>3</sup> for the results presented. A similar approach is hinted by Mikulik *et al.* (2018). The corresponding MOS capacitor is shown in Figure 3.6.

The outcome of the simulation was dependent of the gate voltage range. The voltage range of (-6.0,0.0) V was chosen such that the potential with charge inversion was in the middle of the range. The simulation gives the total charge per cm at every applied voltage point. A partial derivative  $\partial Q/\partial V$  allows to plot C-V. The surface potential can be accessed by measuring the electrostatic potential at the semiconductor-oxide interface as a function of applied  $V$ , transcribing the values at  $x,y = (0,0)$ . A 1D-slice is implemented at the corresponding coordinates ( $x = 0$ , on a slice of 2 nm depth) [10].

In order to plot the curves for different insulators (dielectrics), the SiO<sub>2</sub> thickness can be scaled to an equivalent oxide thickness ( $d_{eq}$ ) by expressing the SiO<sub>2</sub> thickness relative to the new insulator permittivity:  $d_{eq} = d_{SiO_2} \frac{\epsilon_{(SiO_2)}\epsilon_0}{\epsilon_{(insulator)}}$  [13, 44, 45].



**Figure 3.6:** Implemented MOS capacitor for the simulation in the NextNano software package.

### 3.4 Lifetimes measurements

First, lifetimes were to be determined by photoluminescent decay measurements. The device used is a LED-based PL system by greateyes (LumiSolarCell System). The setup is very user friendly. The samples were simply be placed on the stage and the integration

times were adjusted incrementally, starting from 1 s up to 60 s. The light source was 660 nm light source, hence far enough from the bandgap of silicon such that the silicon bandgap transitions can be excluded.

The detected PL signal was very small even with long integration times. Hence a anti-reflection filter was used in order to access the tail of the signal.

Another attempt was made with a system from SemiLab (WT-2000), operating with microwaves, detecting the photoconductance decay carrier lifetimes. The sample is lifetime-mapped with a laser wavelength of 904 nm. However, due to diverse technical discrepancies, the the system is not able to give absolute lifetimes, but serves still to give a relative lifetime comparison between sample regions.



## 4.1 Fabrication of the samples

### 4.1.1 SCIL fabrication and etch parameters

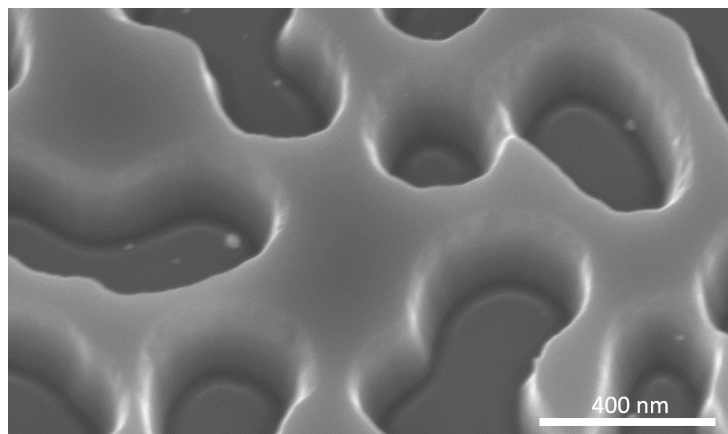
The SCIL process was very straight forward and easily assimilated. Nevertheless, small errors can occur at every step and every sample should be checked on depth and quality before further processing. Figure 4.1 shows one unsuccessful imprint, where the edges are not sharp and the etching seems to have rounded the corners. This could be due to insufficient solgel height after spin-coating for example. As a consequence, the break-through etch of 120 s might be too long, leaving the edges already rounded and exposing facets that would be etched quicker during the direction selective Si etch with HBr.

The etch parameters were defined as 120s  $\text{CHF}_4$  + 40s HBr/ $\text{O}_2$  + 90s HF after having done a HBr time comparison of 70 and 40 s. 40 s HBr silion etching yielded around  $240 \pm 20$  nm depth for the 20  $\mu\text{m}$  and 500  $\mu\text{m}$  silicon and was chosen as the standard etch time for all the samples. The depths were determined by mean of tilted SEM images ( $30^\circ$ ). The HF times were studied in a 1% HF dip series as shown in Figure 4.2, increasing the time from 45 to 105 s (a-d). The pattern wasn't influenced by the dipping neither in aspect ratio, nor in edge quality. Apparently, 40 s HF dip is enough to remove all the solgel. As the silicon doesn't seem influenced by the HF step, longer HF times were maintained such that no residual solgel was risked if during spin-coating the layers resulted thicker for example.

The 10 and 20  $\mu\text{m}$  silicon samples that were bonded to a carrier wafer, were more difficult to image. More charging of the surface made it harder to have a good image acquisition. Furthermore, since the carrier wafers were larger than the imaged 500  $\mu\text{m}$  samples and spanned often over two carbon tape pieces for fixation. This resulted in important drift as the residual elastic deformation in the tape was relaxing. Nevertheless, the depth and quality of the HUD pattern were perfectly reproduced on the thin-Si wafers.

### 4.1.2 Passivation of the samples

Imaging of the passivated layers was used only for occasional quality control. In Figure 4.3 a sample with 250 nm  $\text{Si}_3\text{N}_4$  is shown. The deposition of  $\text{SiN}_x$  is novel for this PECVD setup and the deposition of thin layers needs to be further explored. Namely, the increasing deviation in refractive index with decreasing layer thickness suggests that the deviation in stoichiometry might increase and the optical properties no longer are guaranteed.



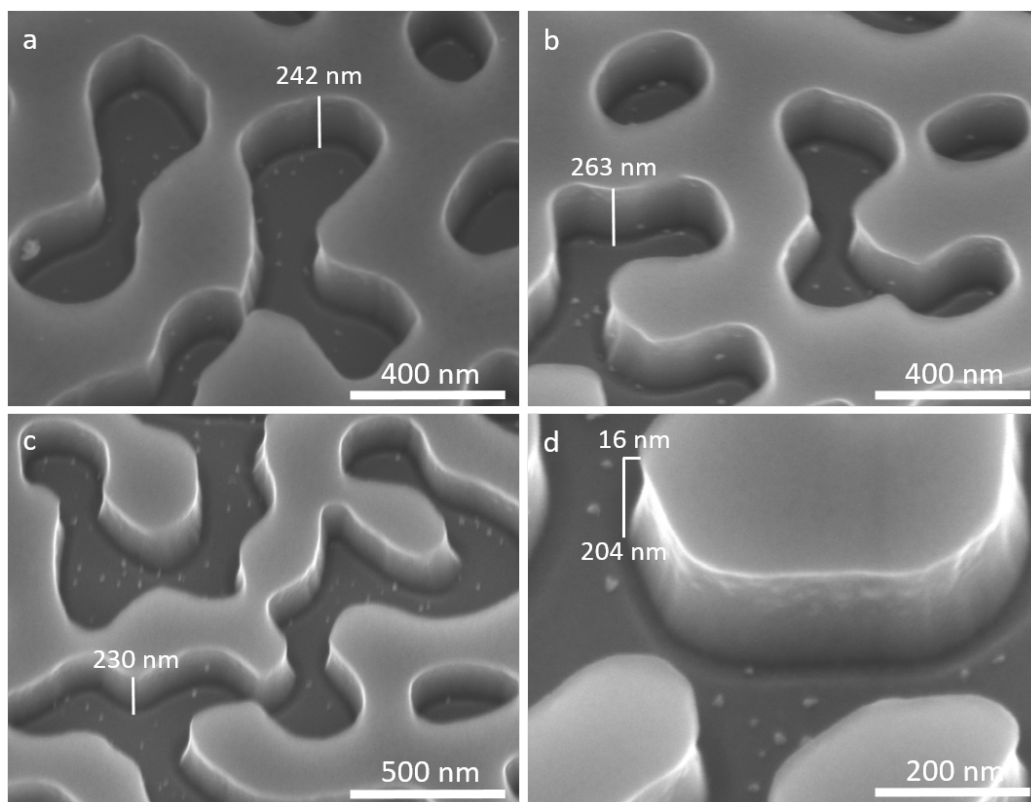
**Figure 4.1:** Unsuccessful spinodal pattern after SCIL imprint of a 500  $\mu\text{m}$  Si sample and etch process: 120s  $\text{CHF}_4$  + 40s  $\text{HBr}/\text{O}_2$  + 90s  $\text{HF}$ .

The relatively thick  $\text{Si}_3\text{N}_4$  layer resulted clearly in a greenish appearance (appendix Figure 6.5). The handling of the ALD system was as well straight forward. However, the system needed often several restarts as it struggled with the connection to all sensors and control devices. The passivation of thin-Si samples was a bit trickier. It was apparent that 20  $\mu\text{m}$  Si samples, that were bonded by PMMA to the carrier wafer, as well as the water bonded samples would start to levitate under the influence of the heat of the chamber and the important air flows of pumping/flushing, displacing them all over the hot plate (appendix Figure 6.5). The ALD chamber isn't in a clean environment and contamination is unavoidable.

The thin wafers were surprisingly resistant to the manipulations and a vast majority survived. Most wafers broke during debonding when surface tensions were involved. That was enough to induce cracks. Grabbing them with tweezers when they were dry, was a rather safe way to handle them.

## 4.2 Optical properties and absorption measurements

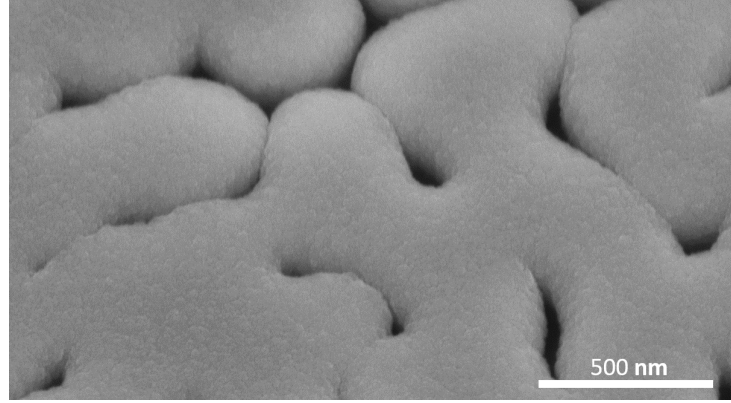
The black body corresponding to 0% reflection was first imitated by a cavity. However, in the setup at hand, back reflection was an issue and the open cavity didn't "absorb" all the light. Tests were done with black tape that was used for beam blocking, too. Indeed, the tape compared to the cavity decreased the reflectance by 100%. When testing perfectly reflective materials for 100% reflectance, the provided white cavity cover was used. However, when measuring it with respect to a silver mirror, only about 85% reflectance were measured. The quality of the white paint was hence much lower than indicated by the provider. That's why the black tape and silver mirror were chosen to



**Figure 4.2:** HF dip series for different times following the standardized etch process: 120s  $\text{CHF}_4$  + 40s  $\text{HBr}/\text{O}_2$ . a) 45 s HF, b) 60 s HF, c) 75 s HF, d) 105 s HF

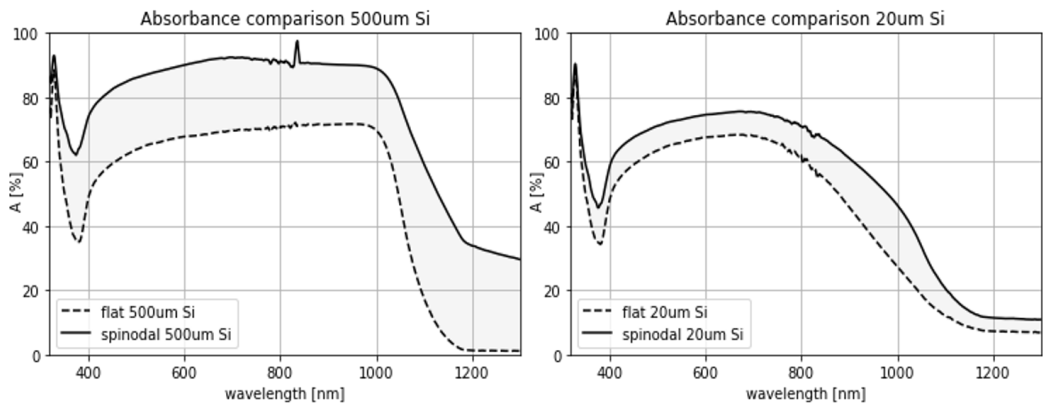
make baseline corrections. The spectral reflectivity data provided by the producer of the mirror was interpolated to match the resolution of the acquired sample data for correction.

The transmission spectrum of the carrier wafers for the was used to correct for thin-Si samples. Figure 4.4 compares the absorbance spectra of spinodal and flat 500  $\mu\text{m}$  (left) and 20  $\mu\text{m}$  (right) silicon samples, unpassivated. The shaded area shows the increase in absorbance due to patterning, accounting for 24.8% and 9.5% for the thick and thin-Si, respectively. The shape of the curve matches Figure 1.3 by Tavakoli *et al.* (2020) and the difference is likely due to the missing ARC coating. The improvement in absorbance due to the HUD patterning is three times bigger for the 500  $\mu\text{m}$  than the 20  $\mu\text{m}$  silicon. A bigger percentage of the back-reflected and trapped light is effectively absorbed in the thicker Si. The influence of 10 nm  $\text{SiO}_2$  or  $\text{Al}_2\text{O}_3$  on the absorbance lies within the error of the equipment, hence the layers are too small to have a significant influence on the optical properties. 10 nm  $\text{SiO}_2$  for example increase the absorbance by 2% for the spinodal,



**Figure 4.3:** Spinodal pattern after SCIL imprint of a 500  $\mu\text{m}$  Si sample and etch process: 120s  $\text{CHF}_4$  + 40s  $\text{HBr/O}_2$  + 90s  $\text{HF}$  and 240 nm PECVD  $\text{Si}_3\text{N}_4$  deposition.

and decreases it by 1% for the flat samples. The measurements are stable and deliver very constant values. This agrees with the results calculated with the Fresnel equations.

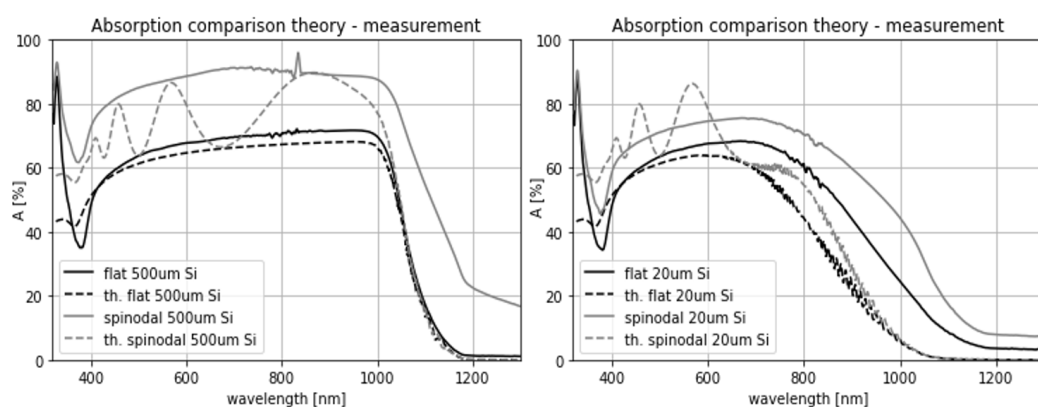


**Figure 4.4:** UV-VIS spectra of flat and spinodal texturing of 260 nm depth and 0.66 filling fraction for 500  $\mu\text{m}$  and 20  $\mu\text{m}$  silicon. The shaded area represents 24.8% and 9.5% for the thick and thin Si, respectively.

Figure 4.5 shows the measured absorbance against theoretical values when implementing the Fresnel equation for a layered stack with a non-polarized beam with normal incidence. The band transition at 1100 nm for silicon is well visible for the 500  $\mu\text{m}$  Si sample. The drop in absorbance in this region is less pronounced for the thin-Si, nevertheless visible. The decreased efficiency in absorbance in the range of 800 - 1000 nm is well distinguished by the flattening curve, when compared to the 500  $\mu\text{m}$  Si. This is in agreement with the moderate absorbance of Si due to its indirect bandgap. When looking

at the spectrum for thin-Si (right), it can be observed that the measured spinodal curve has a clear drop around the bandgap. This is not predicted by the theoretical curve, where the spinodal structure is simply modelled with a uniform refractive index. Hence, the HUD pattern improves the absorption for energies close to the bandgap.

The absorbance, mainly for the thick silicon, doesn't drop to zero for energies lower than the bandgap and predicted by theory (Figure 4.5). This means that reflectance or/and transmittance are overestimated for longer wave lengths. The measured flat silicon spectra agree very well with the results from the online calculator by *Filmetrics* [8]. An example is shown in appendix, Figure 6.6. Hence, the calibration of the setup is correct and the data collected for the HUD samples should be reliable. Furthermore, the 30% of reflection for wavelengths above the bandgap in spinodal samples has been measured for another sample, too. Thus, it is likely not due to the samples alone. This residual reflection (and absorption) is more pronounced in thick than in thin HUD Si. This could be due to the orientation of the light incident on the sample. In transmission mode, the light arrives with  $0^\circ$  angle of incidence and the thickness of the cavity plate might not play any role. In reflection mode, the diffuse light from the integrating sphere should be cancelled out with the baseline correction, whereas the reflected light from the sample might interfere with the thickness of the metallic cavity plate and cause an overestimation of the reflection. The theoretical curves show the interference between the stack of layers, introduced by modeling the HUD by a homogeneous layer (refractive index equation 1.1). The increase of the absorbance due to the spinodal structure agree with Tavakoli *et al.* For the  $20\ \mu\text{m}$  Si, the oscillation follows nicely the measured curve for lower wavelengths. In the region of the band gap, the measured values are much higher than those suggested by calculation, again probably related to the overestimation of reflectance.



**Figure 4.5:** UV-VIS spectra of flat and spinodal texturing of 2400 nm depth and 0.66 filling fraction for  $500\ \mu\text{m}$  and  $20\ \mu\text{m}$  silicon compared to a three layer stack

### 4.3 Surface state density measurements

Electrochemical impedance spectroscopy (EIS) data was collected successfully for native and 10 nm SiO<sub>2</sub> passivated spinodal and flat 500  $\mu\text{m}$  silicon. A piece of 10  $\mu\text{m}$  silicon was successfully etched with HF and bonded to a Al-covered silicon wafer. This was the only sample that was measured with the setup shown on Figure 3.3 on the right. All other samples have been tested with the mounting system on the left. Several measurement cycles were conducted on 500  $\mu\text{m}$  samples and the results were reproducible in terms of magnitude of  $C^{-2}$ , however a voltage shift in the order of  $10^{-2}$  V was observed. This is within the variation of the open circuit potential.  $E_{OC}$  was always subject to variation, although mostly steady at the order of  $10^{-2}$  V. This was the case for two different electrodes tested. Once it averaged to  $-0.36 \pm 0.01$  V over 90 s of measurement time. Another time it was steady at  $-0.55 \pm 0.03$  V with a decreasing tendency before the measurement. After the measurements it was verified and found to be  $-0.38 \pm 0.01$  V. Whereas the measured capacitance was consistent, the effective voltage, although expressed with respect to the substrate, might be subject to some offset in the order of  $10^{-2}$  V.

The IV curve measured for annealed 10 nm Al<sub>2</sub>O<sub>3</sub> on Si showed that outside the range of  $(-1.2, +0.2)$  V with respect to Ag/AgCl (V vs.  $E_{OC}$ ), there would be leakage current and strong hydrogen evolution for more negative voltages. However, when performing single frequency measurements at 100 kHz, no depletion was visible in this region. Indeed, on the search of the limit of the system, a decrease in capacitance could be observed between 2.0 and 4.1 V vs.  $E_{OC}$ . This range even seemed variant, as for several measurements it was shifted by about 0.8 V. Generally, the range of no net current found by I-V measurements, wasn't coherent with the EIS measurements. The range needed to be readjusted for every run.

As for 10 nm Al<sub>2</sub>O<sub>3</sub> (annealed) + 250 nm Si<sub>3</sub>N<sub>4</sub> covered silicon, the IV curve showed no leakage current in the range of  $(-0.6, +0.4)$  V vs.  $E_{OC}$ . When EIS measurements at 100 kHz were performed, a drastic decrease in capacitance seemed to occur in a small voltage range around 3.4 or 4.0 V vs. the reference electrode, if the measurement was rebooted at these voltages. However, if the range was adjusted such that the apparent depletion region was entered by increasing voltage, then no decrease in capacitance was observed anymore. Probably this is due to the charging of the surface and oxide capacitance that happens incrementally, forming the space charge region. If high voltages are applied directly, then the charge carriers in the surface layers couldn't follow fast enough. This agrees with what has been observed when the system got stuck; When the measurements were rebooted at the same voltage, not the same capacitance was measured. There was actually an off-set in the order of  $10^{-2}$  V, indicating that the surface capacitance first needs to charge.

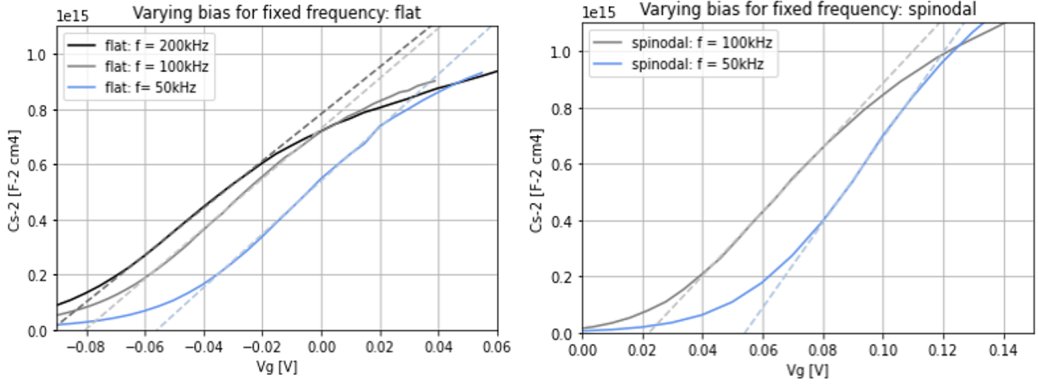
Figure 4.6 shows the  $C^{-2}$ -V curves for two single frequency measurements (50 and 100

kHz) for flat and spinodal 500  $\mu\text{m}$  Si with native oxide. For high negative potentials, the substrate surface is in accumulation and no space charge regions are present. There the capacitance corresponds to the passivation and interfacial oxide layer [44]. For both, the capacitance is lowest at  $0.03 \mu\text{Fcm}^{-2}$ . The minimum capacitance for spinodal 500  $\mu\text{m}$  Si with native oxide and native + 10 nm  $\text{SiO}_2$  is for both 0.02. The same is shown in Figure 4.7 for a full multi-frequency measurement 1-100 kHz for additionally 10 nm  $\text{SiO}_2$  passivated silicon. The capacitance increases ( $C^{-2}$ -V decreases) as the voltage increases and the space charge region broadens. The order of magnitude of the capacitances found agrees with literature [27, 28, 44]. As the surface goes through depletion, a large dispersion of the curves is observed. At higher frequency, the capacitance increases ( $C^{-2}$  decreases) at lower bias. This behavior is in agreement with Meng *et al.* (2017), indicating a high density of interface traps. Furthermore, they report as well a characteristic bump due to charging/discharging of interface traps that hence contribute to the capacitance. This cannot be observed in any of the measured curves. Chen *et al.* (2012) suggest that the dispersion, approaching the accumulation region, is due to bulk-oxide traps. The bumps they observe in the inversion region closer to depletion, do not have any frequency-dependent dispersion and are hence associated with surface traps [6]. A similarly large dispersion is observed for all the samples.

Using the Mott-Schottky equation, the doping density  $N_d$  and flatband potential  $V_{fb}$  have been extracted for the multi-frequency measurements. The numerical values for 1 and 100 kHz are reported in Table 4.1. The tendencies are visualized in Figure 4.8 for  $N_d$  on the left side, and for  $V_{fb}$  on the right side. For the flatband potential, the trend is clear. With increasing frequency, the flatband potential is decreasing for all the samples, flat and spinodal, with and without additional  $\text{SiO}_2$ . The fact that there's a frequency dependence indicates the high density of surface states for all the samples. Low-frequency measurements were performed at shorter intervals and it's visible, that in this region, the flatband potential drops quicker. For low frequencies, the surface charges have time to respond and influence the Fermi level of the semiconductor. For high frequencies on the other hand, they are more immobilized and the flatband potential stabilizes. The slopes seem very similar and no conclusion can be made about the evolution of the density of states between the samples.

When looking at the evolution of the density of dopants (left), for all but the spinodal with additionally  $\text{SiO}_2$  the number increases. As stated by Zhang *et al.* (2007), the bigger the slope, the fewer surface states and the smaller the depletion region [45]. The slopes are all very similar, with the flat Si passivated with  $\text{SiO}_2$  being a bit steeper towards high frequencies. Hence the passivation might reduce the amount of surface states. The spinodal + native oxide has the lowest doping density, indicating a lower density of surface states.

For the maximum frequency attainable with the potentiostat at hand (200 kHz), the change of  $N_d$  and  $V_{fb}$  was slower, however no plateau was yet reached. The frequency, at



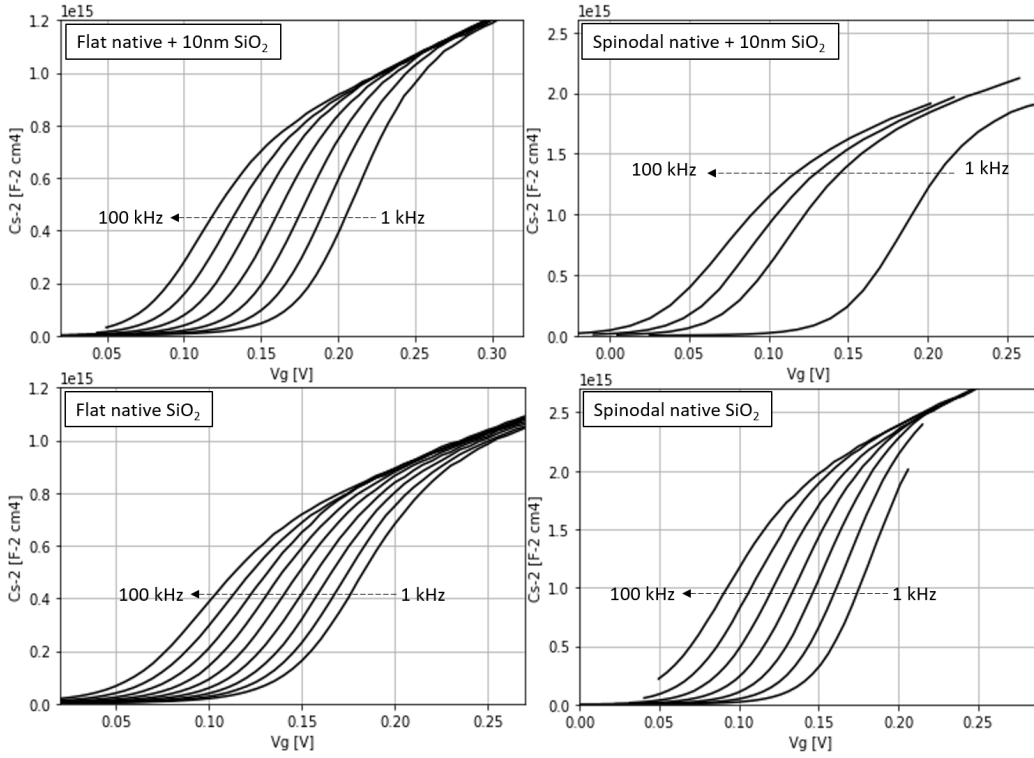
**Figure 4.6:**  $C^{-2} \text{ cm}^{-2}$  vs. bias measurements for different frequencies and surface textures (left: flat, right: spinodal) obtained with EIS. The dashed lines are the tangents of the depletion regions of the MOS capacitors.

which the defects couldn't follow anymore, wasn't reached yet. Therefore, frequencies up to 1 MHz are mostly used. Nevertheless, at 100 kHz the total capacitance is nearly frequency independent and free from the contribution of traps, which is in agreement with [6].

The order of magnitude of the doping density seems reasonable with the indicated (large!) resistivity range of 1-20  $\Omega$  and corresponds to the silicon of the thinned-down solar cells.

The surface texture and aspect-ratios change a lot between the thick dielectric layer of  $\text{SiN}_x$  and the thinner oxide layers. Capacitive differences might be expected due to defects and altered interaction between the dielectric and electrolyte interface. However, as a consequence of the of the highly concentrated (saturated) KCl solution, the Debye length is very small. Any possible capacitance would be much larger than the oxide capacitance. Defects at the passivation layer-KCl interface are localized adjacent to the solid-liquid interface and hardly influence the MOS capacitance [27]. This makes EIS with electrolyte contacts a very stable method for high-aspect ratio structures.

The setup at hand had some limitations. Due to a technical issue, the potentiostat or software were stopping at random moments of the measurement and most multi-frequency cycles couldn't be completed. This didn't change when varying the amount of measurement points, voltage range, etc. As discussed above, there was a voltage off-set after rebooting and the curves couldn't be patched together. Further, the reported wide voltage ranges [6, 25, 27] couldn't be reached with this setup. This is shown in Figure 6.7 in the annex, where the full range of -1.5 V to 0.5 V vs. the reference electrode is shown. Strong hydrogen evolution was the consequence if exceeding the narrow V-range. The zoom-in shows the range studied for example in Figure 4.7. The surface was damaged due to important hydrogen evolution and it was a rather slow process to look for the



**Figure 4.7:** Multi-frequency EIS measurements of 500  $\mu\text{m}$  Si samples with flat (left) and spinodal (right) surface;  $C^{-2}$  vs. gate voltage (applied- $E_{OC}$  for a frequency range of 1-100kHz. Upper row: native + 10 nm of  $\text{SiO}_2$ , lower row: native  $\text{SiO}_2$ . The gate voltage  $V_g$  is with respect to the substrate.

depletion voltage range without exceed it excessively. Finally, the instability of the open circuit potential made the measurements somewhat unreliable.

## 4.4 Minority carrier lifetimes measurement

The photoluminescence lifetime mapping didn't give any significant signal for integration times between 1 and 60 s. Several samples have been tested, passivated, patterned and thick/thin ones, without any difference. Afterwards a quick test was done on a standard silicon wafer from the lab, covered with 6 nm  $\text{Al}_2\text{O}_3$  and annealed at 600  $^{\circ}\text{C}$  after a standard RCA1, RCA2 clean. An expected silicon response was registered and thus the functionality verified. After the insertion of the filter, used to filter out the reflection that might be dominating the weak PL signal, still no response from the samples was found.

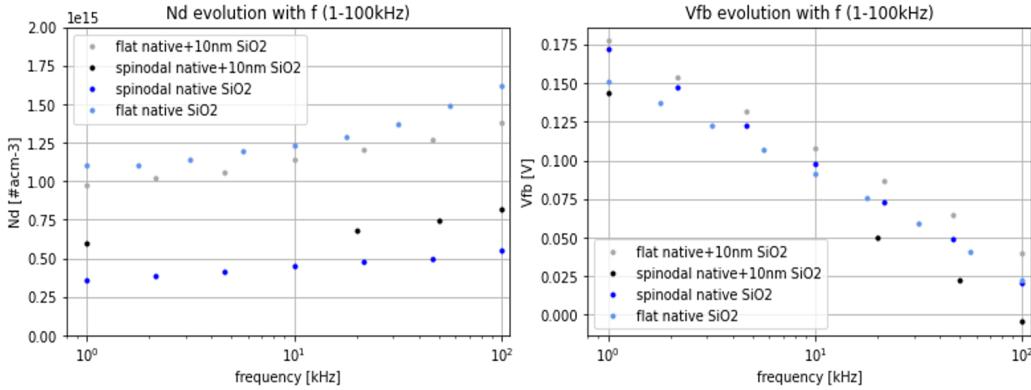
A photoconductance lifetime mapping was therefore attempted. The resulting color

frequency (kHz)	texture	passivation	$N_d$ [ $\#a/cm^3$ ]	$V_{fb}$ [mV]
100	flat	native SiO <sub>2</sub>	$1.62 \cdot 10^{15}$	0.02
1	flat	native SiO <sub>2</sub>	$1.10 \cdot 10^{15}$	0.15
100	spinodal	native SiO <sub>2</sub>	$5.55 \cdot 10^{14}$	0.02
1	spinodal	native SiO <sub>2</sub>	$3.60 \cdot 10^{14}$	0.17
100	flat	10 nm SiO <sub>2</sub>	$1.38 \cdot 10^{15}$	0.04
1	flat	10 nm SiO <sub>2</sub>	$9.72 \cdot 10^{14}$	0.18
100	spinodal	10 nm SiO <sub>2</sub>	$8.21 \cdot 10^{14}$	0.08
1	spinodal	10 nm SiO <sub>2</sub>	$1.10 \cdot 10^{15}$	0.19

**Table 4.1:** Flatband potential ( $V_{fb}$ ) and doping density ( $N_d$ ) determination with the Mott-Schottky equation 1.8 from EIS data collected for flat and spinodal 500  $\mu m$  silicon samples for different frequencies. The flatband potential is given with respect to the substrate.

scale image shown in Figure 4.9 doesn't give access to absolute lifetime values. A relative comparison between samples is however possible. Figure 4.9 shows the lifetime map obtained via photoconductance decay measurements for low lifetimes in the order of 1 ms. Samples 1.-4. are 500  $\mu m$  flat Si samples with passivation layers: 10 nm SiO<sub>2</sub>, native oxide, 10 nm Al<sub>2</sub>O<sub>3</sub> (annealed), 10 nm Al<sub>2</sub>O<sub>3</sub> (annealed) + 250 nm Si<sub>2</sub>N<sub>3</sub> (increasing order). No relevant difference in lifetimes is visible. Samples 5.-8. are 500  $\mu m$  spinodal Si samples with passivation layers: 10 nm SiO<sub>2</sub>, 10 nm Al<sub>2</sub>O<sub>3</sub> (annealed), 10 nm Al<sub>2</sub>O<sub>3</sub> (annealed) + 250 nm Si<sub>2</sub>N<sub>3</sub>, native oxide (increasing order). On samples 5. and 6. a hint of a decrease in lifetimes for the patterned area can be made out. Over all, they seem to have a decreased lifetime compared to the 1.-4. Contrarily, sample 7. couldn't be distinguished from the unpatterned reference samples. Sample 8, which is a native oxide covered spinodal sample, has overall higher lifetimes (even higher than the underlying commercial IBC solar cell) and has as well a hint of decreased lifetimes in the spinodal area. This agrees with the observation from EIS data, that the number of dopants is lowest for this sample (Figure 4.8), indicating reduced interface trap states. However, as the used wafer had a large resistivity range, the sample could simply be a wafer region with lower doping concentration. 9.& 10. are 20  $\mu m$  Si samples with native silicon, flat and spinodal, respectively. They seem to have lifetimes in the same order of samples 5. and 6.

The silicon samples with  $N_d$  in the order of  $10^{15} cm^{-3}$  are moderately doped and the intrinsic bandgap is reduced [30]. The PL spectrum is shifted to lower energies and might not be detected sufficiently anymore. However, with the added filter even very low intensities should have been detected. The conclusion is, that the lifetimes are very short. The operator denoted them "dead". The laser of the CL equipment has a wavelength of 904 nm, which corresponds to a penetration depth of 3.6  $\mu m$  in silicon (37 % of it's initial intensity). Hence the method is surface selective and should be adapted for the 20  $\mu m$  silicon samples, too. It is thus coherent, that the thin-Si samples show similar lifetimes as

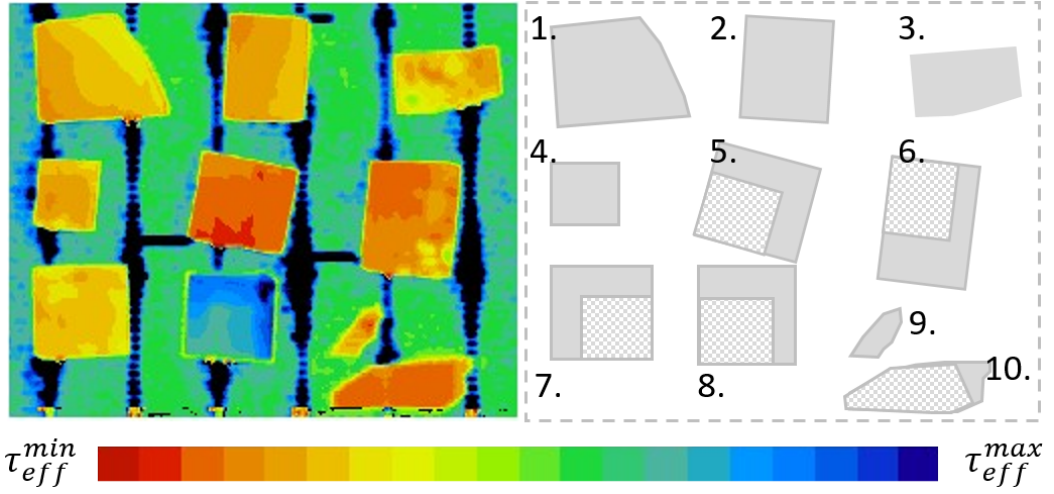


**Figure 4.8:** Evolution of the number of dopants  $N_d$  (left) and the flatband potential  $V_{fb}$  (right) with respect to changing measurement frequency, extracted from the Mott-Schottky plots on Figure 4.7 and 4.6, using equation 1.8.

the thick-Si, if both have a similar surface quality, composition, or contamination. The PL images are not conclusive and no coherent tendency is observed.

The spinodal samples all underwent HF etching and had thus had their surface contamination and native oxide thoroughly removed. The spinodal sample that has just regrown its native oxide at the surface after the removal by HF, might have the highest effective lifetimes because its surface contamination is minimal. On the other hand, the samples that had been passivated afterwards might have suffered heavier contamination than anticipated throughout the process and have a great decrease in lifetimes.

This brings new importance to contamination control and the importance of cleaning. The native oxide was not removed before the deposition of additional passivation layers. The native oxide has proven beneficial for the initiation of the growing layers and the good quality interface with the silicon. The PECVD process is initiated by a  $O_2$  plasma clean, which activates the surface simultaneously. However, the samples have already been inspected by SEM in an uncontrolled environment. As it comes to the ALD samples, the surface has not been activated by plasma as recommended, which might induce defects. Furthermore, with the purpose of having the same conditions for the thin and thicker Si wafers, the systematic RCA1/RCA2 clean was skipped for the reasons that it altered the etching parameters due to surface modification and that the thin wafers were too prone to breakage. This is definitely sub-optimal in order to avoid surface trap states.



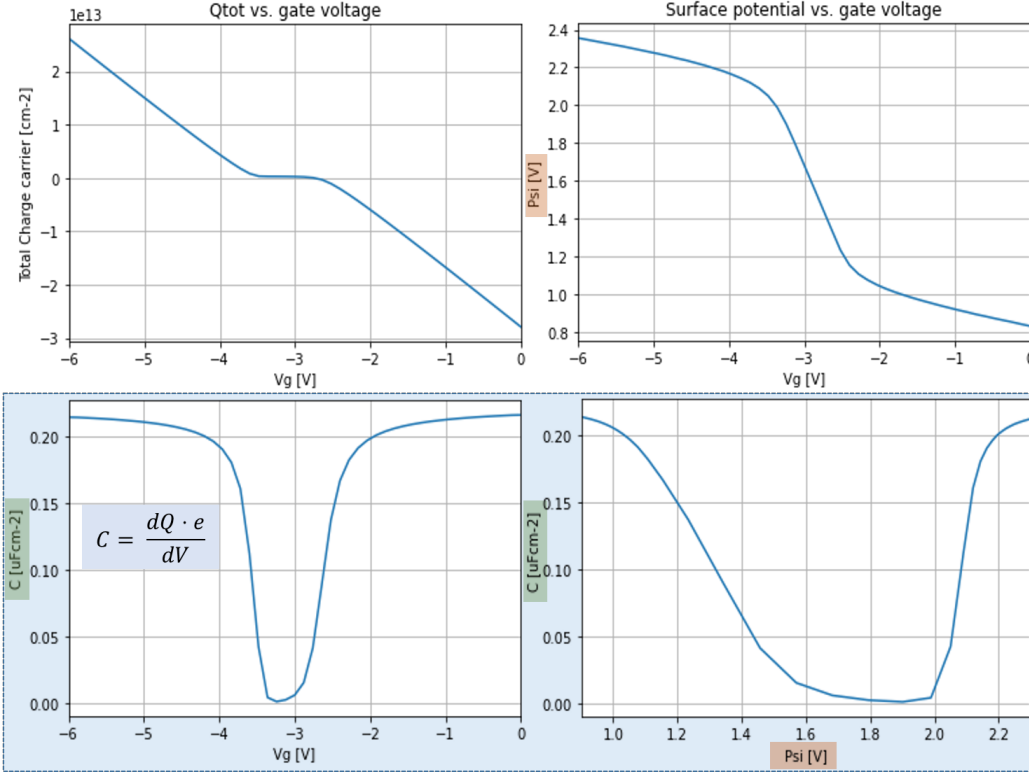
**Figure 4.9:** Relative lifetime map obtained via photoconductance decay measurements for low lifetimes in the order of 1 ms. (1.-4.) 500  $\mu\text{m}$  flat Si samples with passivation layers: 10 nm  $\text{SiO}_2$ , native oxide, 10 nm  $\text{Al}_2\text{O}_3$  (annealed), 10 nm  $\text{Al}_2\text{O}_3$  (annealed) + 250 nm  $\text{Si}_3\text{N}_4$  (increasing order). (5.-8.) 500  $\mu\text{m}$  spinodal Si samples with passivation layers: 10 nm  $\text{SiO}_2$ , 10 nm  $\text{Al}_2\text{O}_3$  (annealed), 10 nm  $\text{Al}_2\text{O}_3$  (annealed) + 250 nm  $\text{Si}_3\text{N}_4$ , native oxide (increasing order). (9.& 10.) 20  $\mu\text{m}$  Si with native silicon, flat and spinodal, respectively. The figure on the right is a draft where the spinodal areas are highlighted by the texture. The corresponding photograph can be found in the appendix (Figure 6.5).

## 4.5 Terman method and NextNano

A major focus was on understanding how to quantitatively compare the EIS measurements. Therefore, figuring out how to apply the high-frequency Terman method merited some attention. It was very surprising that, although very widely used, no one provided the ideal curves used for the comparison with the measured ones. Neither was it explained, how to simulate them, i.e. what parameters have been used. It remains a black box still. This gives insights in how reporting has changed with the granted access to databases and simulation tools. Detailed information appears to be superfluous. This is in contrast to the work by Goetzberger *et al.* (1966), who published a collection of  $\Psi_s$ -V curves, because the access to data wasn't granted. Calculating ideal data isn't simple because many parameters of the material need to be known beforehand. Chen *et al.* (2012) for example adapted the Schottky-barrier height (gate work function) such that the it crossed over the 1-MHz data at the inversion point in the depletion region. Hence, assuming the 1-MHz as quasi-ideal, as the trap states can't follow the high frequency.

Extracting the relation between surface potential and capacitance was therefore done with the NextNano software package for only one case, namely 10 nm  $\text{SiO}_2$  on n-type

silicon. The results are shown in Figure 4.10. The graphs in the top row, i.e.  $Q_{tot}$  vs.  $V_g$  and  $\Psi_s$  vs.  $V_g$  were directly extracted from the simulation. The total charge carriers designates the amount of charge carriers ( $-p+n$ ) per cm of substrate, hence are multiplied by the substrate thickness and divided by the area in order to get coherent units with the EIS data. The graphs in the lower row have afterwards been calculated from the two above.



**Figure 4.10:** Results of the NextNano simulation for a n-type silicon with doping density of  $10^{15}\text{cm}^{-3}$  for a MOS capacitor like represented in Figure 3.6, including a  $\text{SiO}_2$  layer of 10 nm thickness. The top row ( $Q_{tot}$  vs.  $V_g$  and surface potential  $\Psi_s$  vs.  $V_g$ ) are extracted directly from the simulation, the lower row ( $C$  vs.  $V_g$  and  $C$  vs.  $\Psi_s$ ) are obtained by differentiation of the  $Q_{tot}$  vs.  $V_g$  plot. The  $C$  vs.  $\Psi_s$  plot can be used as an ideal plot for the high-frequency Terman method, not including any interface trap states.

The surface potential  $\Psi_s$  and the capacitance are both in the right order of magnitude [13, 28]. These ideal curves represent roughly the flat 500  $\mu\text{m}$  silicon sample with native  $\text{SiO}_2$ . However, capacitance range of the simulation ( $0.0\text{--}0.2\ \mu\text{Fcm}^{-2}$ ) is roughly 3x smaller than the measured one ( $0.0\text{--}0.6\ \mu\text{Fcm}^{-2}$ , appendix Figure 6.8). Considering that the native oxide is thinner than the assumed 10 nm, the simulated capacitance is even overestimated. A superposition like in the ideal case shown in Figure 3.5 is definitely not yet possible.

This underlines the difficulty to obtain representative curves, as the real MOS capacitor can deviate largely from the ideal case. The high-frequency method is indeed not preferred for not being very accurate. Compared to the high-low frequency method, it's more prone to errors. All the methods are based on fitting and separating capacitances. Furthermore, the doping profile needs to be known as exactly as possible, which is one of the unknowns or can only be approximated through the Mott-Schottky approach for example. Due to non-uniform charge distribution along the interface with the oxide could alter the calculated surface capacitance. There, EIS is beneficial because of the large and good contact area of the electrolyte with the high-aspect ratio surface structure. Furthermore, true high-frequency curves need to be measured. In the case of 100-200 kHz, it has been discussed above, that this frequency might not be high enough yet in order to avoid the contribution from interface states [31].

With the purpose of showing the efficiency of surface passivation approaches on high aspect ratio HUD thin-Si solar cells, the process has been broken down into three main steps: 1) Comparing the most common surface passivation techniques on 500  $\mu\text{m}$  Si, patterned and flat. 2) Repeat some of the approaches on 10, 20 and 30  $\mu\text{m}$  Si wafers, patterned and flat. 3) Reproduce the most promising recipes on thinned-down IBC Si solar cells. The optical properties were tested by UV-VIS. The minority charge carrier lifetimes with PL measurements. The presence and density of surface trap states was assessed by implementing EIS characterization. The pattern and surface quality was verified by SEM. The HUD structures were produced with a Substrate Conformal Imprint Lithography (SCIL) process, facing all the perks of handling brittle and lightweight thin-silicon wafers. The surface passivation techniques used were atomic layer deposited (ALD)  $\text{Al}_2\text{O}_3$  and a-SiN<sub>x</sub> and a-SiO<sub>2</sub> evaporated via plasma enhanced chemical vapor deposition (PECVD).

All the fabrication and characterization steps have been failed, adapted and tested successfully on thick and thin Si samples. For 500  $\mu\text{m}$  Si samples, one generation of samples has been fabricated and characterized successfully. PL minority charge carrier lifetime measurements result in very low lifetimes, suggesting important contamination. This is in agreement with the large dispersion of the Mott-Schottky plots in the depletion region measured by EIS, which is a sign for many surface states and fixed oxide charges. A strong frequency dependence of the flatband potential and doping density has been observed for all the samples, including the flat 500  $\mu\text{m}$  Si sample covered with native oxide. It's low lifetimes for a moderately n-doped silicon suggest that the initial wafer batch might already have been issue to contamination. A HF-etched sample with regrown native oxide showed the highest lifetimes. The qualitative comparison of the PL and EIS data didn't allow to identify any trends in the effect of passivation on flat and patterned samples.

The quantitative evaluation of the EIS data requires a set of ideal capacitance vs. surface potential curves for every doping concentration and oxide thickness. Even though a lot of work is based on the so called *Terman* method, the origin or the generation of such idealized curves remains a black box. First attempts have been undertaken to generate these with the NextNano software package.

A series of passivation techniques has been done on 20  $\mu\text{m}$  Si samples. Due to time restrictions they have not yet been bonded to a conductive substrate (Al-covered silicon) in order to back-contact them in EIS measurements. The process of HF-etching a thin-Si

wafer one-sided and water-bond it to the conductive substrate has been tested successfully. Consecutively, EIS has been performed and the process has been validated.

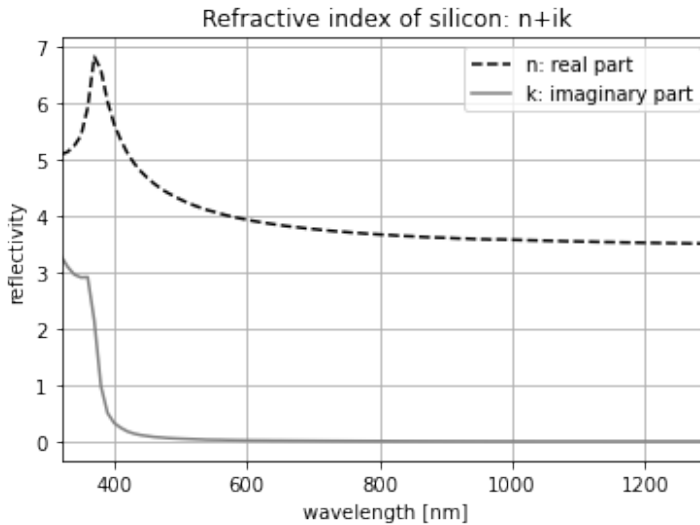
Initially, the main focus should have been on the surface passivation of the samples. Besides that the SCIL procedure was only ready to manufacture samples in the last third of the project, much time was as well needed to make the characterization techniques operational for silicon samples. Whereas EIS has not been performed yet within the group, many issues took time to resolve. This includes the malfunctioning of the potentiostat in multi-frequency measurements. Technical support should have been sought directly in order to accelerate the data acquisition. The UV-VIS measurements needed to be adapted, too, as the standard procedures used by other operators weren't compatible with the samples at hand. After many discussions it was concluded, that no silicon compatible laser/detector equipment was available on site and that the PL measurements needed to be done externally. Due to the sanitary situation, their organization was very slow and inflexible.

It was eye-opening to experience the lead times for highly specialized products. A drawn conclusion is, that the implementation of a research project is very time consuming. A period of six months for a project abroad, where the techniques and scientific knowledge need to be initially acquired, is very short. Let alone, if everything is slowed down by the current sanitary situation. In this context, it would have been even more important to discuss issues and further steps on a daily basis as.

As a follow-up, the 20  $\mu\text{m}$  Si samples should be bonded and analyzed with EIS. As for the 500  $\mu\text{m}$  Si samples, a new batch and passivation series should be produced and characterized. Special attention should be paid to external contamination and a standard RCA1/RCA2 procedure should be done before any passivation step. Regardless of the thin-Si sample handling. With the soon-to-arrive HF vapor equipment, the cleaning and native oxide removal will be facilitated enormously for thin-Si samples. For the characterization, a quantitative comparison of EIS data will need to suffice at first. Combined with results from PL, the high-frequency method can be applied for a selected amount of samples with generated ideal curves. With the setup at hand, low-frequency data cannot be generated and hence the other methods cannot be used. An interesting alternative could be the implementation of the conductance method, which works great for high aspect ratio structures and is estimated to deliver more precise results. Instead of working with the difference between capacitances, the conductance is measured and directly related to the interface traps. The methods at hand are compatible with the thinned-down solar cells in terms of handling and temperature and should be easily adapted.

It could be interesting to study the surface of the passivated structures with AFM in order to determine the surface quality. Trials led to the breakage of the tips, hence the correct parameters need to be studied first.

## Introduction



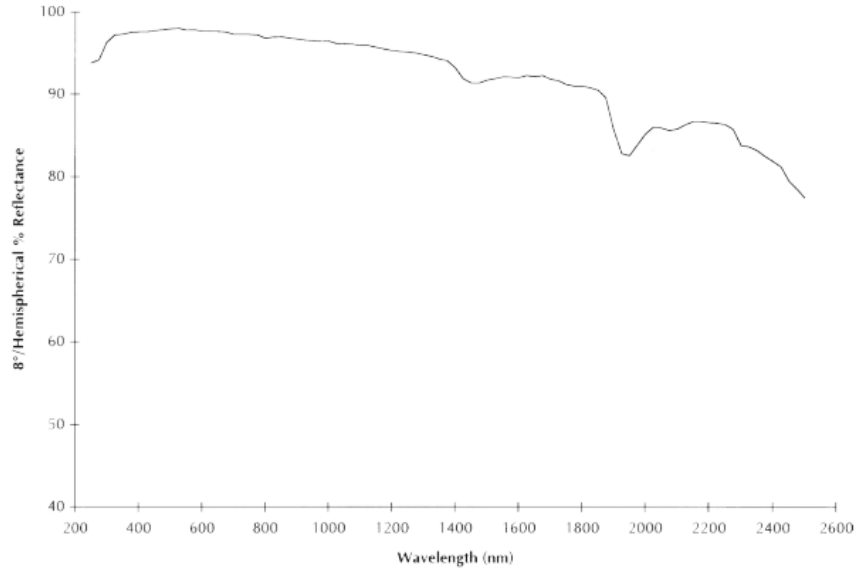
**Figure 6.1:** Complex refractive index of silicon, based on data from Schinke *et al.* (2015) [1]

## Methods

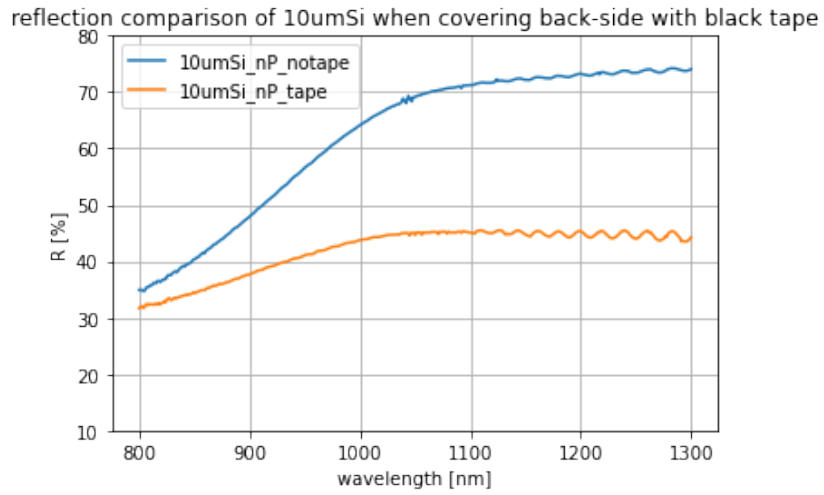
### Filling fraction determination with ImageJ

In order to determine the filling fraction of the spinodal pattern, SEM image were analyzed with the freeware ImageJ. First, images are converted into 16-bit type >Image>Type>16-bit. Then the coloring was adjusted in order to get a two-color image >Image>Adjust>Threshold. Then the areas of both colors can be compared >Analyze>Set Measurements, tick "Area", "Area fraction" and "Display label". To start the analysis >Analyze>Measure. The areal fraction of the, in the case of Figure 6.4, red area is calculated.

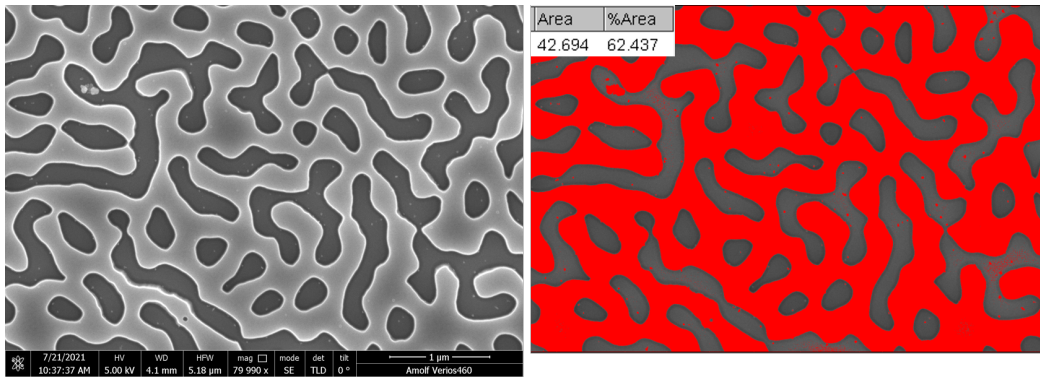
## Results



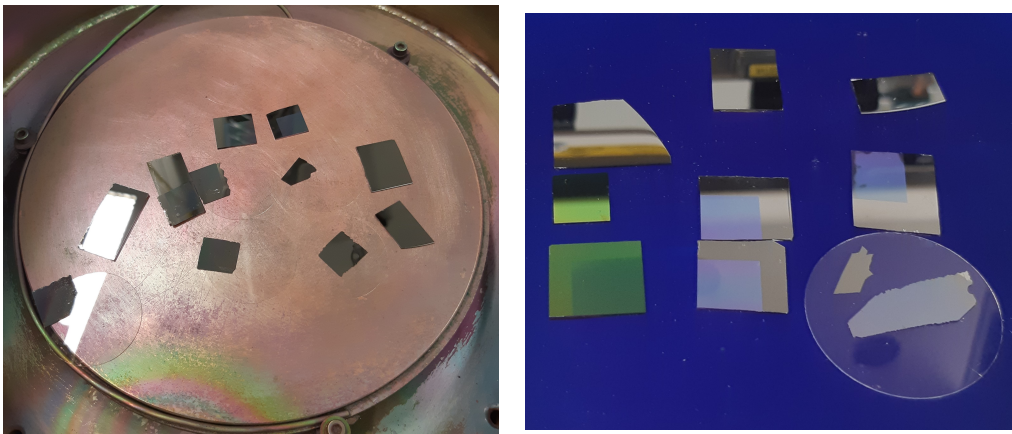
**Figure 6.2:** Spectral reflectance of *Spectrafect* 97% Diffuse Reflectance Coating [22].



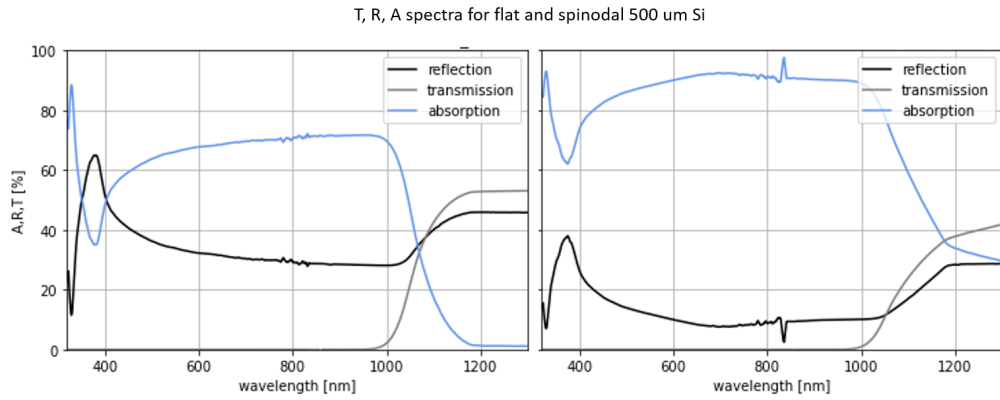
**Figure 6.3:** Reflectance spectrum of 10  $\mu\text{m}$  thin-Si piece bonded to a microscopic slide. By adding a black tape adjacent to the slide, the reflectance decreases significantly for energies below the bandgap. This is the method chosen for reflectance measurements for thin-Si samples.



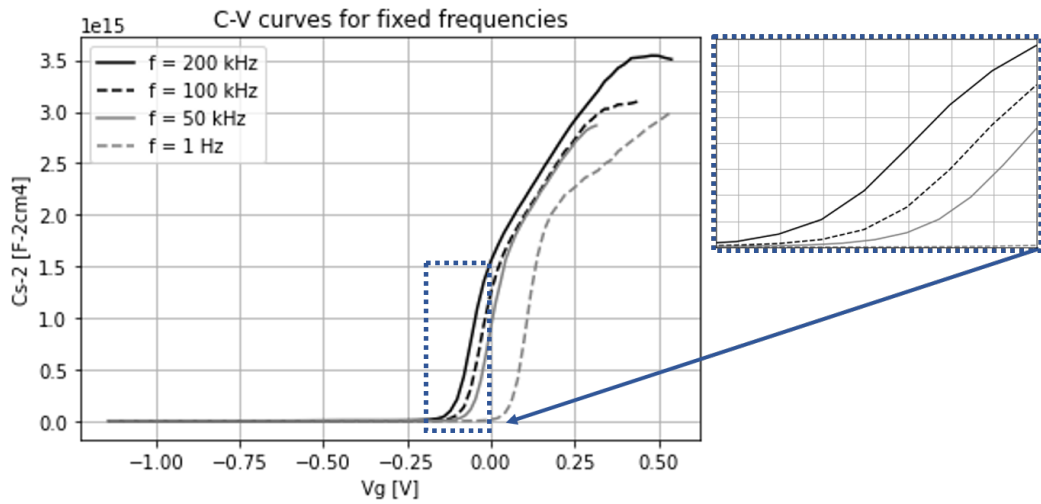
**Figure 6.4:** Analysis of the filling fraction of the HUD pattern using the freeware ImageJ.



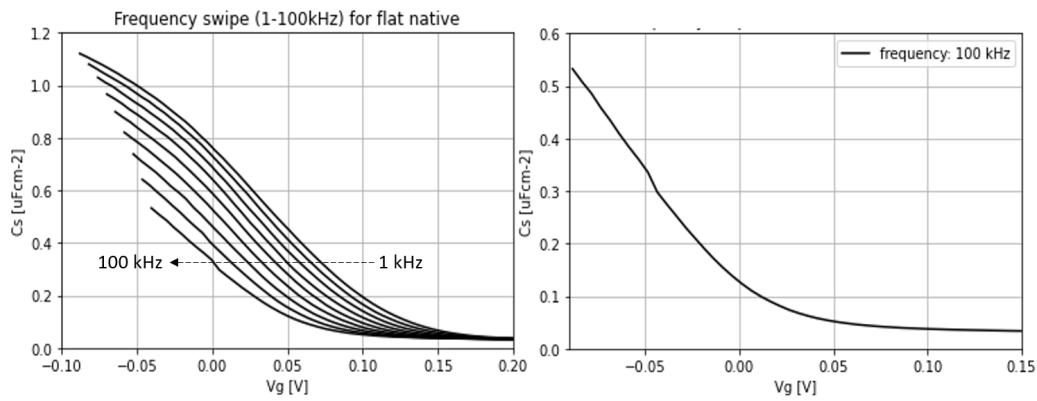
**Figure 6.5:** Sample overview of thin and thick Si, bonded and debonded. Left: ALD hotplate after alumina deposition. The 20  $\mu\text{m}$  samples were debonded under the influence of the heat and levitated freely by means of the airflow in the chamber. Right: Samples for PL measurements.



**Figure 6.6:** Transmittance, Reflection (measured) and Absorbance (calculated) spectra of flat (left) and spinodal (right) 500  $\mu\text{m}$  silicon.



**Figure 6.7:** Flat 500  $\mu\text{m}$  Si in large voltage range measurement and important hydrogen evolution. Zoom-in into range of interest in other EIS measurements.



**Figure 6.8:** Multi-frequency C-V curves (left) and C-V curve for 100 kHz high-frequency measurement for flat 500  $\mu\text{m}$  silicon with native oxide.



# Bibliography

---

- [1] Schinke et al. 2015. *Refractive index database*. 2021. URL: <https://refractiveindex.info/?shelf=main&book=Si&page=Schinke> (visited on 08/08/2021) (see page 49).
- [2] RK Ahrenkiel. **Measurement of minority-carrier lifetime by time-resolved photoluminescence**. *Solid-State Electronics* 35:3 (1992), 239–250 (see page 16).
- [3] Sayak Bhattacharya, Ibrahim Baydoun, Mi Lin and Sajeew John. **Towards 30% power conversion efficiency in thin-silicon photonic-crystal solar cells**. *Physical Review Applied* 11:1 (2019), 014005 (see pages 2–4).
- [4] Stefan Birner, Tobias Zibold, Till Andlauer, Tillmann Kubis, Matthias Sabathil, Alex Trellakis and Peter Vogl. **Nextnano: general purpose 3-D simulations**. *IEEE Transactions on Electron Devices* 54:9 (2007), 2137–2142 (see page 29).
- [5] Howard C Card. **Aluminum–Silicon Schottky barriers and ohmic contacts in integrated circuits**. *IEEE Transactions on Electron Devices* 23:6 (1976), 538–544 (see page 30).
- [6] Han-Ping Chen, Yu Yuan, Bo Yu, Jaesoo Ahn, Paul C McIntyre, Peter M Asbeck, Mark JW Rodwell and Yuan Taur. **Interface-State Modeling of InGaAs MOS - From Depletion to Inversion**. *IEEE transactions on electron devices* 59:9 (2012), 2383–2389 (see pages 27, 39, 40).
- [7] Zhi Chen, Dae-Gyu Park, Francke Stengal, S Noor Mohammad and Hadis Morkoç. **Metal-insulator-semiconductor structures on p-type GaAs with low interface state density**. *Applied physics letters* 69:2 (1996), 230–232 (see page 27).
- [8] Filmetrics A KLA Company. *Filmetrics spectra calculator*. 2021. URL: [https://www.filmetrics.com/reflectance-calculator?wmin=200&wmax=1000&wstep=1&angle=0&pol=s&units=nm&mat\[\]=Air&d\[\]=0&mat\[\]=SiO2&d\[\]=5&mat\[\]=Si&d\[\]=500000&mat\[\]=Air&d\[\]=0&sptype=r](https://www.filmetrics.com/reflectance-calculator?wmin=200&wmax=1000&wstep=1&angle=0&pol=s&units=nm&mat[]=Air&d[]=0&mat[]=SiO2&d[]=5&mat[]=Si&d[]=500000&mat[]=Air&d[]=0&sptype=r) (visited on 17/08/2021) (see page 37).
- [9] Andres Cuevas, Thomas Allen, James Bullock, Yimao Wan, Di Yan and Xinyu Zhang. **Skin care for healthy silicon solar cells**. In: *2015 IEEE 42nd Photovoltaic Specialist Conference (PVSC)*. IEEE. 2015, 1–6 (see pages 8, 12).
- [10] nextnano GmbH Daryoush Nosraty Alamdary. *MOS Capacitor & MOSFET in 2D Tutorial*. 2020. URL: [https://www.nextnano.com/dokuwiki/doku.php?id=nnp:mosfet\\_in\\_2d](https://www.nextnano.com/dokuwiki/doku.php?id=nnp:mosfet_in_2d) (visited on 15/08/2021) (see pages 29, 30).
- [11] Dimitrios Deligiannis, Vasileios Marioleas, Ravi Vasudevan, Cassan CG Visser, René ACMM van Swaaij and Miro Zeman. **Understanding the thickness-dependent effective lifetime of crystalline silicon passivated with a thin layer of intrinsic hydrogenated amorphous silicon using a nanometer-accurate wet-etching method**. *Journal of Applied Physics* 119:23 (2016), 235307 (see page 6).
- [12] K Gelderman, L Lee and SW Donne. **Flat-band potential of a semiconductor: using the Mott–Schottky equation**. *Journal of chemical education* 84:4 (2007), 685 (see page 16).

- [13] A Goetzberger. **Ideal MOS curves for silicon**. *Bell System Technical Journal* 45:7 (1966), 1097–1122 (see pages 30, 45).
- [14] Anna Hankin, Franky E Bedoya-Lora, John C Alexander, Anna Regoutz and Geoff H Kelsall. **Flat band potential determination: avoiding the pitfalls**. *Journal of Materials Chemistry A* 7:45 (2019), 26162–26176 (see page 16).
- [15] Muhammad Badar Hayat, Danish Ali, Keitumetse Cathrine Monyake, Lana Alagha and Niaz Ahmed. **Solar energy—A look into power generation, challenges, and a solar-powered future**. *International Journal of Energy Research* 43:3 (2019), 1049–1067 (see pages 1, 2).
- [16] Wen-Jeng Ho, Po-Hung Tsai, Yi-Yu Lee and Chia-Min Chang. **Electrical and optical properties of thin film silicon solar cells with sub-wavelength surface structure and TiO<sub>2</sub> passivation**. *Vacuum* 118 (2015), 64–68 (see page 10).
- [17] Bram Hoex, Jan Schmidt, P Pohl, MCM Van de Sanden and WMM Kessels. **Silicon surface passivation by atomic layer deposited Al<sub>2</sub>O<sub>3</sub>**. *Journal of Applied Physics* 104:4 (2008), 044903 (see pages 6–9, 11, 20).
- [18] Paris IEA. *Renewable Power*. 2020. URL: <https://www.iea.org/reports/renewable-power> (visited on 05/08/2021) (see page 1).
- [19] Friederike Kersten, Alexander Schmid, Stefan Bordihn, Jörg W Müller and Johannes Heitmann. **Role of annealing conditions on surface passivation properties of ALD Al<sub>2</sub>O<sub>3</sub> films**. *Energy Procedia* 38 (2013), 843–848 (see page 9).
- [20] Ping Kuang, Sergey Eyderman, Mei-Li Hsieh, Anthony Post, Sajeev John and Shawn-Yu Lin. **Achieving an accurate surface profile of a photonic crystal for near-unity solar absorption in a super thin-film architecture**. *ACS nano* 10:6 (2016), 6116–6124 (see page 5).
- [21] M Kuhn. **A quasi-static technique for MOS CV and surface state measurements**. *Solid-State Electronics* 13:6 (1970), 873–885 (see page 27).
- [22] Labsphere. *Spectrafect Diffuse Reflectance Coatings*. 2021. URL: <https://www.labsphere.com/labsphere-products-solutions/materials-coatings-2/coatings-materials/spectralect/> (visited on 09/08/2021) (see page 50).
- [23] JR LaRoche, J Kim, JW Johnson, B Luo, BS Kang, R Mehandru, Y Irokawa, SJ Pearton, G Chung and F Ren. **Comparison of Interface State Density Characterization Methods for SiO<sub>2</sub>/4 H SiC MOS Diodes**. *Electrochemical and Solid State Letters* 7:2 (2003), G21 (see page 27).
- [24] Zhaoheng Ling, Jian He, Xiaoyong He, Mingdun Liao, Peipei Liu, Zhenhai Yang, Jichun Ye and Pingqi Gao. **Excellent passivation of silicon surfaces by thin films of electron-beam-processed titanium dioxide**. *IEEE Journal of Photovoltaics* 7:6 (2017), 1551–1555 (see page 10).
- [25] Anna Dalmau Mallorquí, Esther Alarcón-Lladó, Ignasi Canales Mundet, Amirreza Kiani, Bénédicte Demaurex, Stefaan De Wolf, Andreas Menzel, Margrit Zacharias and Anna Fontcuberta i Morral. **Field-effect passivation on silicon nanowire solar cells**. *Nano Research* 8:2 (2015), 673–681 (see pages 10–12, 40).

- [26] Inès Massiot, Andrea Cattoni and Stéphane Collin. **Progress and prospects for ultrathin solar cells**. *Nature Energy* 5:12 (2020), 959–972 (see pages 1–4).
- [27] Andrew C Meng, Kechao Tang, Michael R Braun, Liangliang Zhang and Paul C McIntyre. **Electrochemical impedance spectroscopy for quantitative interface state characterization of planar and nanostructured semiconductor-dielectric interfaces**. *Nanotechnology* 28:41 (2017), 415704 (see pages 13, 15, 27, 39, 40).
- [28] Dmitry Mikulik, Andrew C Meng, Riad Berrazouane, Josua Stückelberger, Pablo Romero-Gomez, Kechao Tang, Franz-Josef Haug, Anna Fontcuberta i Morral and Paul C McIntyre. **Surface Defect Passivation of Silicon Micropillars**. *Advanced Materials Interfaces* 5:20 (2018), 1800865 (see pages 3–5, 13–15, 27, 39, 45).
- [29] Colorado National Renewable Energy Laboratory Golden. *Best Research-Cell Efficiencies*. 2017. URL: <https://www.nrel.gov/pv/index.html> (visited on 07/08/2021) (see page 2).
- [30] Hieu T Nguyen, Di Yan, Fan Wang, Peiting Zheng, Young Han and Daniel Macdonald. **Micro-photoluminescence spectroscopy on heavily-doped layers of silicon solar cells**. *physica status solidi (RRL)–Rapid Research Letters* 9:4 (2015), 230–235 (see pages 16, 42).
- [31] Edward H Nicollian, John R Brews and Edward H Nicollian. **MOS (metal oxide semiconductor) physics and technology**. Vol. 1987. Wiley New York, 1982 (see pages 13, 15, 27–29, 46).
- [32] Santosh Pandey and S Kal. **A simple approach to the capacitance technique for determination of interface state density of a metal–semiconductor contact**. *Solid-State Electronics* 42:6 (1998), 943–949 (see page 27).
- [33] PerkinElmer. *LAMBDA 750 UV/Vis/NIR spectrophotometer from PerkinElmer brochure*. 2020. URL: [https://resources.perkinelmer.com/lab-solutions/resources/docs/BRO\\_LAMBDA-750-UV-Brochure.pdf](https://resources.perkinelmer.com/lab-solutions/resources/docs/BRO_LAMBDA-750-UV-Brochure.pdf) (visited on 11/08/2021) (see page 23).
- [34] Armin Richter, Martin Hermle and Stefan W Glunz. **Reassessment of the limiting efficiency for crystalline silicon solar cells**. *IEEE journal of photovoltaics* 3:4 (2013), 1184–1191 (see page 2).
- [35] Sven Rühle. **Tabulated values of the Shockley–Queisser limit for single junction solar cells**. *Solar Energy* 130 (2016), 139–147 (see page 1).
- [36] Jan Schmidt, Robby Peibst and Rolf Brendel. **Surface passivation of crystalline silicon solar cells: Present and future**. *Solar Energy Materials and Solar Cells* 187 (2018), 39–54 (see page 10).
- [37] Dieter K Schroder. **Carrier lifetimes in silicon**. *IEEE transactions on Electron Devices* 44:1 (1997), 160–170 (see page 6).
- [38] Simon M Sze, Yiming Li and Kwok K Ng. **Physics of semiconductor devices**. John Wiley & sons, 2017 (see pages 6, 13–15, 27, 28).
- [39] Xinyu Tan, Wensheng Yan, Yiteng Tu and Can Deng. **Small pyramidal textured ultrathin crystalline silicon solar cells with double-layer passivation**. *Optics express* 25:13 (2017), 14725–14731 (see pages 1, 10).

- [40] Nasim Tavakoli, Richard Spalding, Pepijn Koppejan, Georgio Gkantzounis, Chenglong Wang, Ruslan Röhrich, Evgenia Kontoleta, A Femius Koenderink, Riccardo Sapienza, Marian Florescu et al. **Over 65% sunlight absorption in a 1  $\mu\text{m}$  Si slab with hyperuniform texture** (2020) (see pages 2, 4, 5).
- [41] Lewis M Terman. **An investigation of surface states at a silicon/silicon oxide interface employing metal-oxide-silicon diodes**. *Solid-State Electronics* 5:5 (1962), 285–299 (see pages 6, 13, 14, 27).
- [42] Ladislav Harmatha—Andrej Vrbický. **Determination of interface trap density in unipolar structures using quasistatic C–V method**. *Journal of Electrical Engineering* 55:3-4 (2004), 95–99 (see page 27).
- [43] Bin Zhang, Yu Zhang, Ridong Cong, Yun Li, Wei Yu and Guangsheng Fu. **Superior silicon surface passivation in HIT solar cells by optimizing a-SiOx: H thin films: A compact intrinsic passivation layer**. *Solar Energy* 155 (2017), 670–678 (see page 8).
- [44] X Zhang, HT Ren, R Li and G Xiang. **Comparison of electrical properties of aluminum oxide thin films on silicon and gallium arsenide substrates grown by atomic layer deposition**. *Surface and Coatings Technology* 228 (2013), S246–S248 (see pages 16, 30, 39).
- [45] Xiaoge Gregory Zhang. **Electrochemistry of Silicon and its Oxide**. Springer Science & Business Media, 2007 (see pages 15, 16, 30, 39).

# Declaration of Authorship

---

I hereby declare that this thesis is my own unaided work. All direct or indirect sources used are acknowledged as references.

Amsterdam, 26th August 2021



---

Jelena Dolecek  
- 248106 -